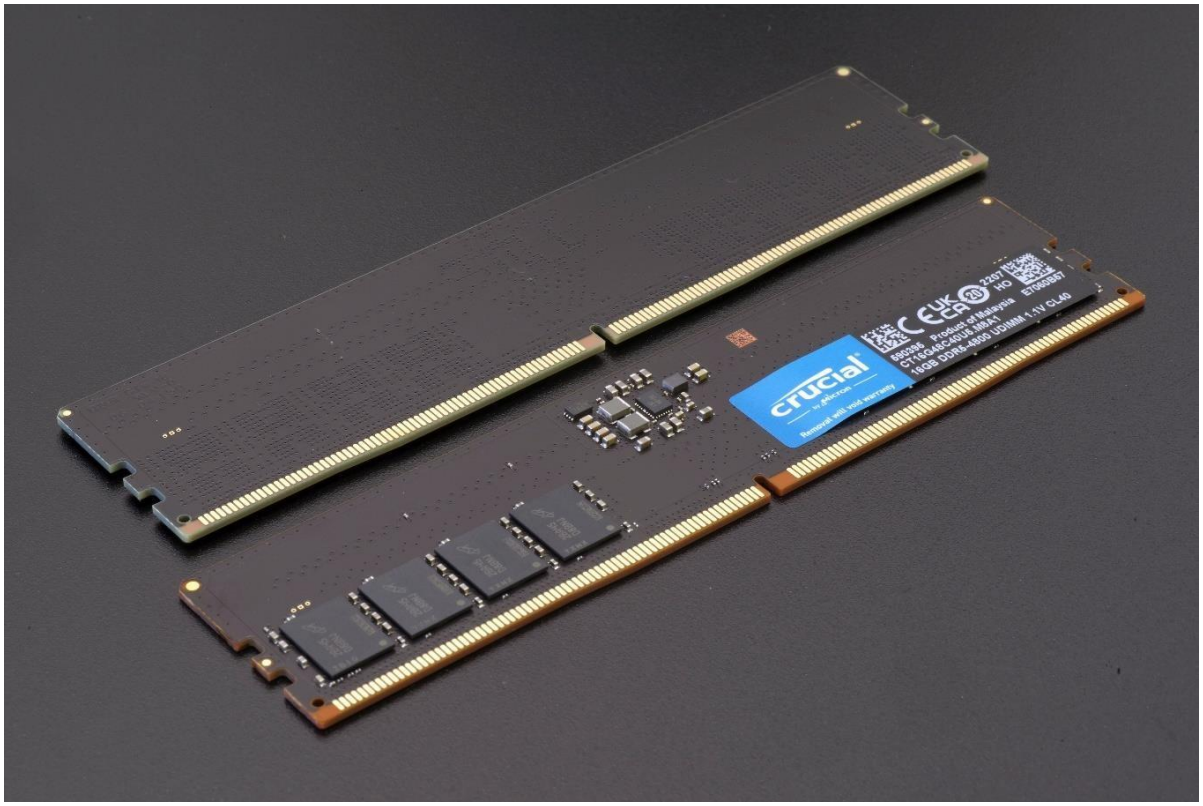
2023



INTRODUCTORY GUIDE TO OVERCLOCKING AND OPTIMIZING DDR-5 ON CHIPSET Z690/Z790

REV 1.03 (07.02.23)

Pakhtunov M.D. (T.ME/PAKHTECH)

Table of contents

Intro. A few words about the guide.

The purpose of writing this guide is to consolidate the information already available, which will be useful for both beginners and advanced overs, in order to facilitate the setup process and in general to get an idea about the subject.
The document will be constantly updated and modernized. All links can be found in the header or in my group @t.me/maxytech

Special thanks to @Anta777, @Garison87, @Olegdjuce, @Odvolk10, @2500K

Revisions

REV 1.01 (11/25/2022)

- Added tachyon to motherboards
- Changes have been made to the "Voltages" section regarding DRAM and CPU VDD2
- Changes have been made to the section “Basic memory testing tools”, added HCI Memtest 7.0

- Changes have been made to the section “Key voltage stability testing tools” added Prime 95

- Added section on JEDEC minimum timings, will be supplemented
- Removed the “Tuning and Matching Process” section until I figure out what to do with it.
- Fixed some bugs and discrepancies in the “Timings” section
- Added an example of tuning for APEX in the “Resistances” section
- Added an example of setting 6800-32 on team groups to the section “Example of reference setting 6800-32-40-40-52”

REV 1.02 (01/29/2023)

- Corrected the current information in the voltage section
- Added additional information on tRFC for Adaev
- Added detailed description for Y-Cruncher
- Added 6666-30 to statistics and comparison with 6800-32 using Teamgroup 6400 1.35V as an example
- Added overclocking of A-DIE Teamgroup 7600 on 12900KS (ADL) + Z690 (UNIFY-X) platform to statistics

- Updated the design

REV 1.03 (02/07/2023)

- All the same as REV 1.02. I made minor changes and remembered the design a little.

Motherboard selection

We consider only two-slot motherboards:

MSI Z690 UNIFY-X (8 layers)

Of the benefits: good overclocking potential (but far from the best), the richest BIOS with various tweaks and settings, monthly microcode updates, rock solid reliability - reliability.

Of the minuses: some tweaks may not work correctly or not work at all; cunning MSI engineers limit the potential of the board, it is necessary to wait for subsequent updates.

What to expect: 6800-32(30), in rare cases 7000-32 on ADL on M-DIE. For RPL and A-DIE, there are few statistics yet.

EVGA Z690/Z790 DARK KINGPIN (10 layers)

One of the best motherboards for overclocking RAM at the moment, on a par with MSI MEG Z690I UNIFY.

Of the benefits: an understandable user-friendly BIOS, high overclocking potential, the ability to manually reduce the RTL block, high reliability.

Of the minuses: relatively high cost, poor functionality, design for an amateur.

What to expect: 6800-32(30), 7000-32(30) CR2/CR1 on ADL on M-DIE. For RPL and A-DIE, there are few statistics yet.

ASUS ROG MAXIMUS Z690/Z790 APEX (8 layers)

Just Apex. Everyone knows. If a successful model comes across, then you are on a horse. If not, selyavi. Lottery.

On the plus side: excellent overclocking potential, if you're lucky. Excellent functionality of the Asus BIOS.

Of the minuses: relatively high cost, a lot of marriage, a successful model may come across, or maybe vice versa. In some revisions, there are problems with one slot.

What to expect: 7000+ on ADL on M-DIE. 7200+ on RPL on M-DIE. There are few statistics for A-DIE yet.

MSI MEG Z690I/Z790I UNIFY (12 layers)

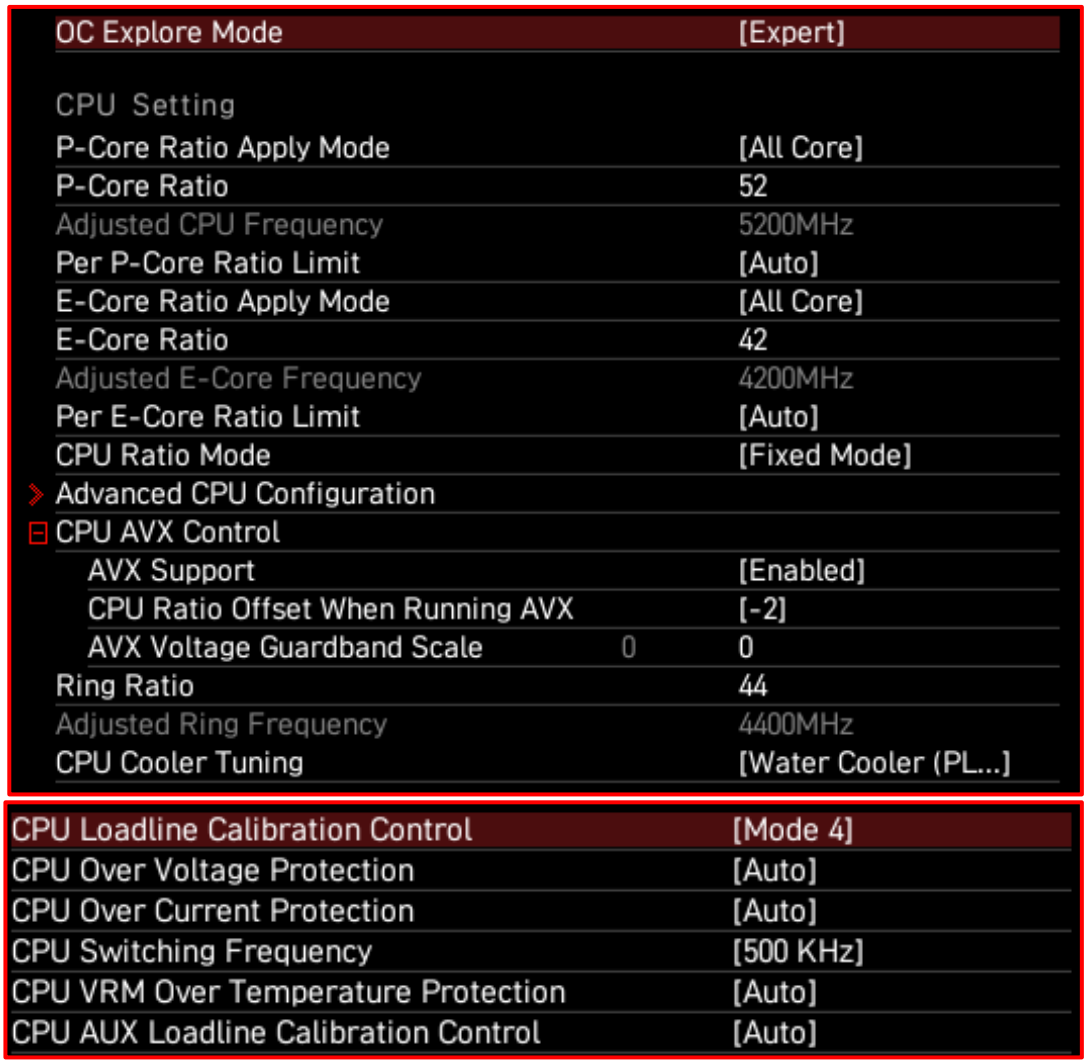
One of the best RAM overclocking boards right now on par with EVGA. Can do what others cannot.

Pros: extremely high overclocking potential. Cons: form factor.

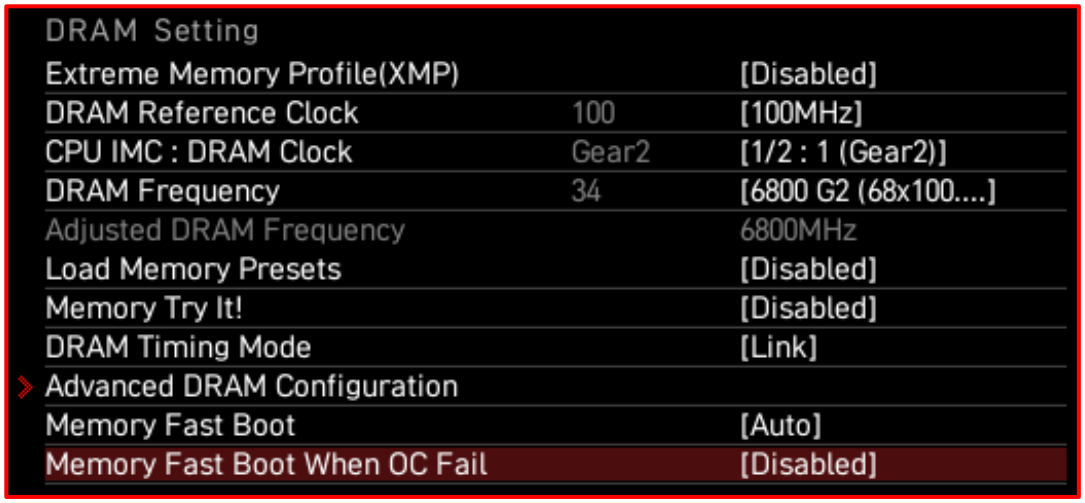
What to expect: 7000+ on ADL on M-DIE. 7400+ on RPL on M-DIE. There are few statistics for A-DIE yet

BIOS presets: Settings, OC

We start by transferring the processor to stock, or we set those settings that have been tested in advance and are 100% stable in order to exclude the influence of the processor.



DRAM Setting- the main block of work with RAM.



Extreme Memory Profile (XMP)

Disabled

DRAM Reference Clock

100MHz / 133MHz.

Essentially, it doesn't matter. When overclocking memory, it is optimal to use a memory multiplier of 133 in the BIOS, and not auto or 100, which will make it possible to create comfortable conditions for the memory controller in the processor and reduce voltages. At the same time, frequencies with a step of 266 - 5866, 6133, 6400, 6666, 6933, 7200 are available.

CPU IMC: DRAM Clock

KP operating mode.
Gear 1: for low frequencies and a “correct” CR-1 Gear 2: basic mode Gear 4: for high frequencies.

DRAM Frequency

Overclocking is best done at JEDEC frequencies in increments of +400: 5600, 6000, 6400, 6800, 7200, 7600

Memory Fast Boot

On MSI boards, you can always leave it in Auto. I choose Slow Training and switch to Auto at the end of the workout.

Memory Fast Boot when OC fail

disabled. When enabled, when overclocking fails, it uses the old stable config. We leave in the car.

>Advanced DRAM Configuration

Memory Force (https://www.msi.com/blog/memory-force)

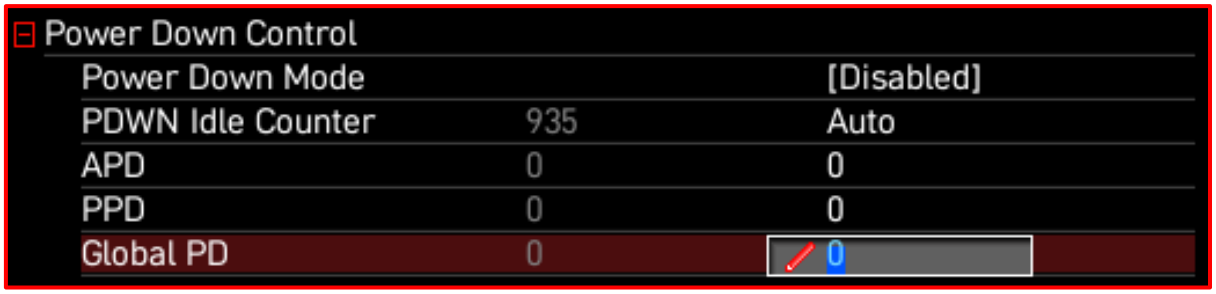
MSI feature, signal of RAM operation in slots. The smaller the strip, the faster the acceleration. Ideally, they should be the same, but even if one is slightly shorter than the other, there is no crime. The signal level can be adjusted by the DRAM VDD/VDDQ voltages.

lucky mode

Always off. This tweak allows you to “trick” the system and achieve higher frequencies at low (and sometimes vice versa) voltages, sacrificing performance. Incorrectly trains and overestimates the RTL block.

Power Down Control

Energy saving. Always off PDWN Idle Counter to Auto.
The very tweak that will allow you to win a couple of ns latency for your RAM.



> DRAM Training Configuration

Everything else is in the car. You can experiment.

SenseAmp Offset Training –**DISABLED** DIMM
ODT Training -**ENABLED** DIMM DFE Training -
ENABLED
Write Drive Strength/Equalization 2D -**ENABLED** VDDQ
Training-**ENABLED** Round Trip Latency -**ENABLED**

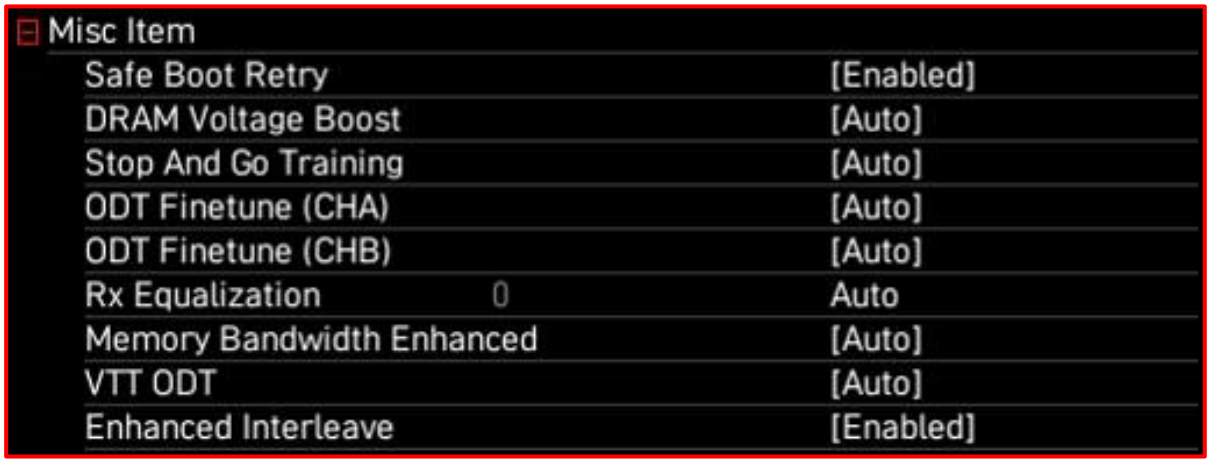
Turn Around Timing Training -**DISABLED**

> DRAM PMIC Features

VDD/VDDQ/VPP Switching Frequencyyou can set to the maximum, everything elseAuto.

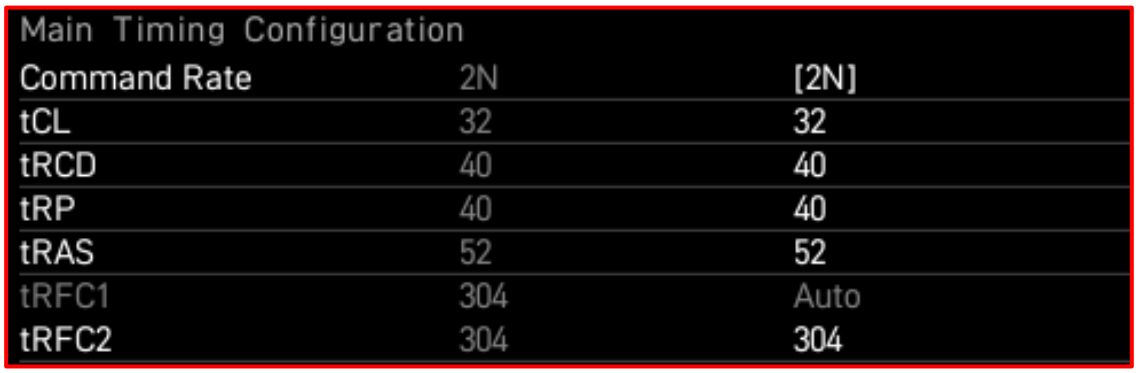
> MISC Item

Enhanced Interleave - Enabled. Improves dual rank performance.



Timings

> Primary (MAIN)



Main Timing Configuration		
Command Rate	2N	[2N]
tCL	32	32
tRCD	40	40
tRP	40	40
tRAS	52	52
tRFC1	304	Auto
tRFC2	304	304

command rate.

Available options on MSI: [2N], [1N], [N:3], [Real 1N]; on EVGA: [2N], [1N]

There are many questions about the correctness of the last three modes. Moreover, there are many questions to the CR1 itself on DDR-5. Therefore, we focus only on [2N]. If you want to be able to work with CR1, then your choice is definitely EVGA.

tCLalways even:28-30-32-34. At frequencies above 6400 MHz, it is optimal to tune the memory to tCL 32 and higher. The reference is tCL 32 up to 7000 inclusive and tCL 34 and above for 7200 and above. tRCD=tRP. Equal to tCL (usually at low frequencies) or in increments of +7, 8, 9, 10, 11, 12.

For a frequency of 6800 and above, I recommend making a minimum step of +8 (32-40-40). +7 (32-39-39) is also working, but requires much higher voltages, and you will hardly see a difference in performance.

32-38-38-50
32-39-39-51
32-40-40-52
32-41-41-53
32-42-42-54
32-44-44-56

tRASwe bet according to the formula and nothing else. In fact, you can put any, but do this not needed, the best option is tRAS=tRCD+tRTP.

tRFC2multiple16 is always set to auto until the memory is fully stabilized. Stability tested by Y-Cruncher N32+N64 test. The limits for DDR-5 are around 300 for

M-DIE: 336, 320, 304, 288. A-DIE:
544, 528, 512, 496, 480

> Secondary (SUB)

Sub Timing Configuration		
tRFCPB	240	240
tREFI	130560	130560
tWR	48	48
tWR_MR	48	48
tWTR	15	Auto
tWTR_L	34	Auto
tRRD	8	8
tRRD_L	8	8
tRTP	12	12
tRTP_MR	12	12
tFAW	32	32
tCWL	30	30
tCKE	8	8
tCCD	8	8
tCCD_L	12	12
tCCD_L_MR	12	12

tRFCPBshould be lowertRFC2 and is also a multiple of 16. Approximate difference between RFC2 and RFCPB according to Jedec 80.

tREFIas well asWe always leave tRFC2 in auto until the memory setup is complete.

Affects temperature. Stability tested by Y-Cruncher N32 test. You can put
absolutely any, but it is better to choose from the values:

262143maximum, no shift **130560**
(shift within2x)
87040(shift within3rd)
65280(shift within only4 x tREFI)
52224(attREFIx9 in BIOS = max =255 there will still be an opportunity to shift the update as conceived within 5xtREFI)

tWR, tWR_MRalways even with step +6. The minimum value is 48. As a rule, it has almost no effect on stability, so**48**- standard.

[tWR=tWR_MR]
[tWR=tWRPRE-tCWL-8]
. . . 72, 66, 60, 54, 48

tWTR, tWTR_Lalways inAuto. Interrelated with tWRRD_sg/dg timings, more on them below. [tWTR=tWTR_L]
Target for tWTR=8-10 (minimum 4), for tWTR_L=16-24 (minimum 16)
[WTRL=WRWRsg] according to JEDEC (since the BIOS always overestimates wtrs and wtrl by 2, this remains with DDR4, then you can set WTRL=WRWRsg-2)

tRRDS=8, tRRDL>=8, but not more than 18 according to JEDEC.

tRTP, tRTP_MRmay be odd, try to put even =12, in some cases 14. [tRTP=tRTP_MR]

tFAW=32 always (ForDDR-5 memory with 1K Jedec pages at any frequency!)

tCWLalways even. [tCWL=tCL-2]. MSI trains in increments of -4. [tCWL=tCL-4]. This option also possible, but not recommended. **tCKE**=8**tCCD**=8

tCCD_L, tCCD_L_MR=18, 16, 14, 12. For a frequency of 6800MHz, the board trains at 17 (5ns=17 cycles). It is better to set even and reduce. The benchmark is this: up to 6800 inclusive **tCCD_L**=12, for 7000 and above tCCD_L=12, 14, 16 [tCCD_L=tCCD_L_MR]

> Tertiary (TURN AROUND TIMING CONFIGURATION)

Turn Around Timing Configuration		
Turn Around Timing Setting Mode		[Fixed Mode]
tRDRDSG	12	12
tRDRDDG	8	8
tRDRDDR	1	1
tRDRDDD	1	1
tWRWRSG	18	18
tWRWRDG	8	8
tWRWRDR	1	1
tWRWRDD	1	1
tRDWRSG	20	20
tRDWRDG	20	20
tRDWRDR	1	1
tRDWRDD	1	1
tWRRDSG	58	58
tWRRDDG	50	50
tWRRDDR	1	1
tWRRDDD	1	1

All tertiary timings give a good increase in copying and recording, but they are also sensitive in tuning - instability is manifested in the compressed timings!

Turn Around Timing Setting Mode -**FIXED**

tRDRDSG [tRDRDSG=tCCD_L=tCCD_L_MR].

tWRWRSG [tWRWRSG=tCCDLx2=tRDRDSG*2=tCCDLWR] Can be reduced to 16.

tRDRDDG=8 always;**tWRWRDG**=8 always;

tRDWRSG=**tRDWRDG**Can be left completelyAuto and reduce by -1 to no boot. Optimal 20, minimum 17-18. At high frequencies 22.

tWRRDSG, tWRRDDG Interesting timings that require additional attention. Interrelated with tWTR, tWTR_L formulas:

tWTRL=tWRRDsg-tCWL-10
tWTRS=tWRRDdg-tCWL-10

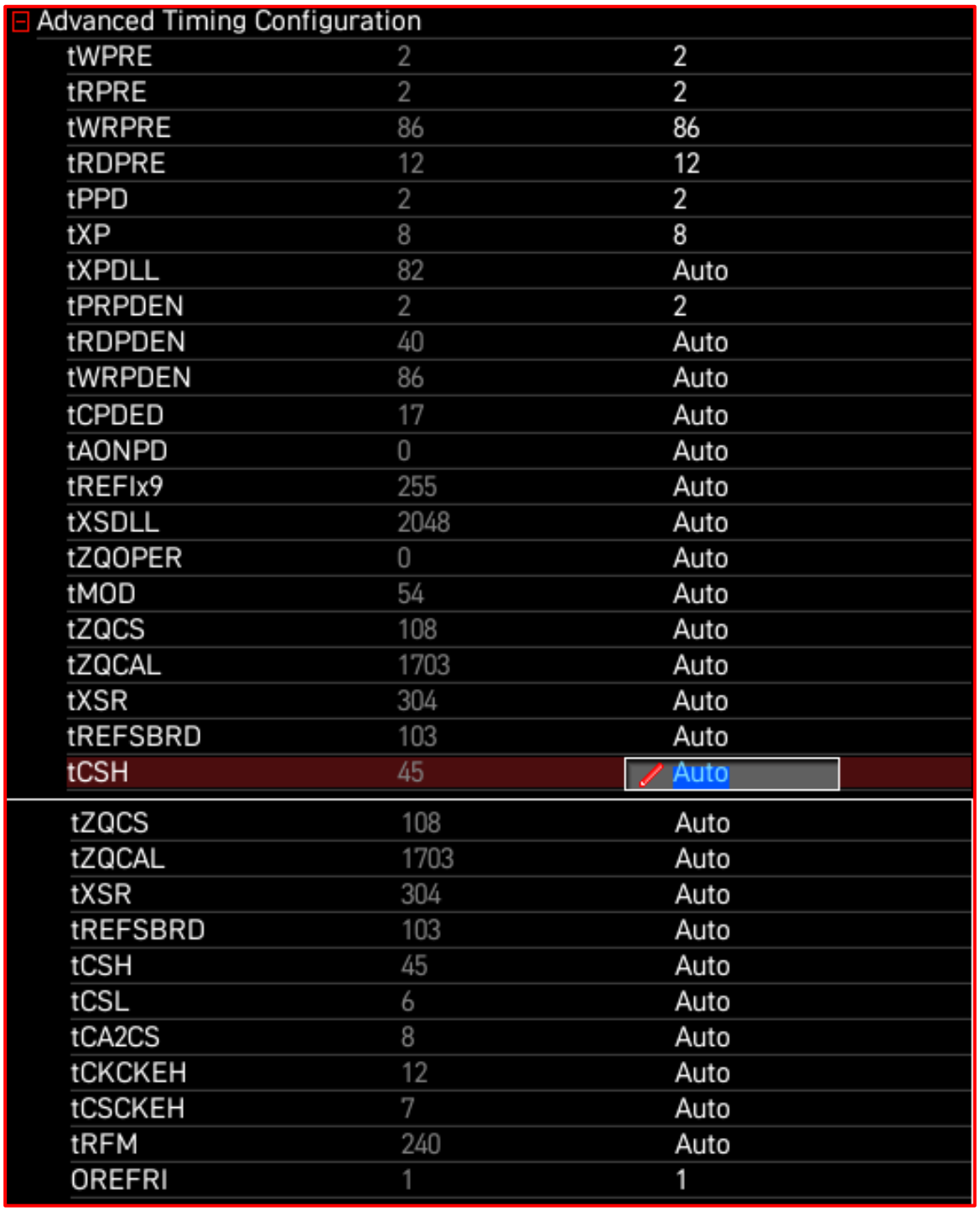
The board gives priority to tWRRDSG, tWRRDDG, therefore, only these two values need to be set in order for the board to train tWTR, tWTR_L, which in turn are always set to auto.

It is necessary to set in auto and reduce by -2. Landmark 62/52, 62/50/ 60/50, 58/50, 58/48, 56/48

ASrock Timing Configurator incorrectly shows tWTR, tWTR_L, in it they are always +4 from the true values. MSI Dragonball solves this problem.

We set all DR / DD timings to ones or zeros if the memory is peer-to-peer. For 2x32 dual ranks, the formulas are:
[RDRDdr=8+RPRE]; [WRWRdr=8+WPRE]; [WRRDdr=6+RPRE] For dr/dd formulas for WRRD are valid for CWL=CL-2

> Advanced (ADVANCED)



Here we touch almost nothing, except for some important timings:

tWPRE=always auto=2
tRPRE=always auto=2

txp=8

tRDPRE

Important! The board can set an odd value, you need to set it manually according to the formula:

[tRDPRE=tRTP]

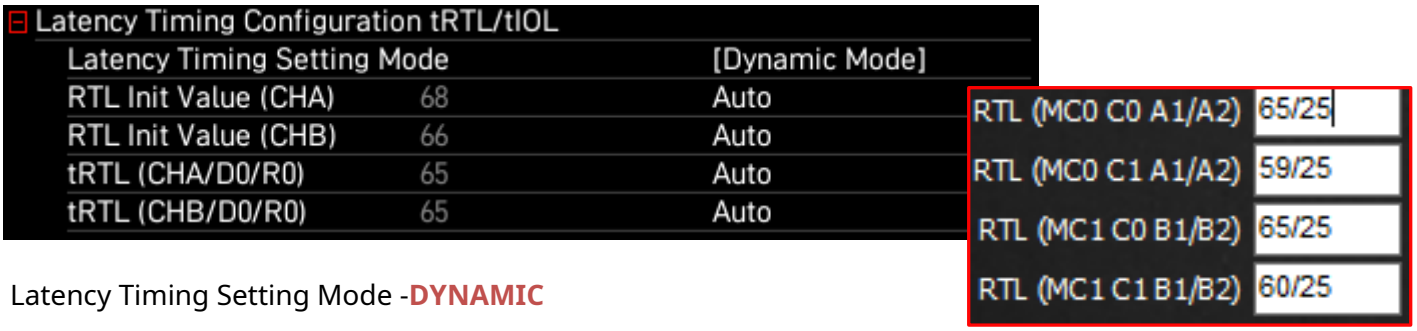
tWRPRE
Can be left in the car.
[tWRPRE=tWR+tCWL+8]

tPRPDEN, tRDPDEN, tWRPDEN, OREFRI
[tPRPDEN=2]; [tRDPDEN=CL+9]; [tWRPDEN=CWL+9+WR]; [OREFRI=1]
Timings related to energy saving.

! Due to the bios timings can be different, and odd, and smaller. This is for all timings, except for tCL and tCWL (they are even for Gear2).

> Latency Timing Configuration tRTL/tIOL (RTL block)

MSI boards should always be set to Auto. The board itself trains this block. Unfortunately, you can't change it like on EVGA boards.



Latency Timing Setting Mode -**DYNAMIC**

Calculation/validation of RTL (look in Asrock Timing Configurator):

For 6800
At tCL=30 RTL=57/58
At tCL=32 RTL=59/60
RTL=memory frequency/800 + tCL + 19 then round down (RTLA) and up (RTLB)

> Minimum JEDEC timings

tWR	48	tPPD	2
tRRDL	8	tCPDED	8
tRRDS	8	tRDRDsg	8
tWTRL	16	tRDRDdg	8
tWTRS	4	tRDWRsg	17
tRTP	12	tRDWRdg	17
tFAW	32	tWRWRsg	16
tCWL	tCL-2	tWRWRdg	8
txp	8		

Voltages

Important !!be sure to read[Buildzoid](#) for the sake of completeness.

CPU SA Voltage Mode		[Auto]
CPU SA Voltage	0.932V	0.930
CPU VDDQ Voltage	1.116V	1.110
CPU VDD2 Voltage	1.380V	1.370
CPU 1.05 Voltage		Auto
CPU 1.8 Voltage		Auto
CPU AUX Voltage	1.816V	1.800
CPU PLL SFR Voltage		Auto
RING PLL SFR Voltage		Auto
SA PLL SFR Voltage		Auto
E-Core L2 PLL SFR Voltage		Auto
MC PLL SFR Voltage		Auto
DRAM Voltage Mode		[Unlink]
DRAM DIMMA1 Voltage	1.425V	1.425
DRAM DIMMB1 Voltage	1.440V	1.440
DRAM DIMMA1 VDDQ Voltage	1.370V	1.370
DRAM DIMMB1 VDDQ Voltage	1.370V	1.370
DRAM DIMMA1 VPP Voltage	1.800V	1.800
DRAM DIMMB1 VPP Voltage	1.800V	1.800
PCH 0.82 Voltage		0.700

Main voltages (DRAM):

DRAM VDDQ (SWB)- maximumJEDEC 1.4V / MSI 1.435V (without unlock 1.4) / HYNIX 1.5V;

DRAM VDD (SWA)- maximumJEDEC 1.4V / MSI 1.435V (without unlock 1.4) / HYNIX 1.5V;

Relatively safe voltages for both:

> without airflow up to1.48V in case with normal air exchange
> Airflow required1.48V-1.56V
> Mandatory water block over1.56V

Also watch the temperature. Anything up to 50 gr. I consider acceptable.

The main voltage responsible for stabilizing the memory is**DRAM VDD (SWA).** It is necessary to reduce DRAM VDDQ (SWB) before instability occurs. And then reduce DRAM VDD (SWA). DRAM VDD (SWA) is less flexible, so ideally DRAM VDDQ < DRAM VDD (but no more than 6% jedek / 4-5% in my personal experience). When manipulating DRAM VDDQ, we do not forget about CPU VDD2, but they must be equal. Should not.

[DRAM VDD = DRAM VDD-3(4)(5)%]

Main voltages (CPU):

CPU SA– range byMSI from 0.6V - 1.6V, border 1.25V. It should also be as low as possible, down to 0.9V, if the processor's KP allows. The limit value is around 1.35V, but**1.25~**should be enough for everything.

CPU VDD2 (IMC VDD)– range byMSI 0.85V - 2.2V, MSI limit 1.44V, it is better not to exceed**1.4**

CPU VDD2- main voltageIMC DDR PHY (physical layer - interface for "communication" of the CP with the memory). You can draw an analogy: DDR-4 - SA and DDR-5 - IO. Affects timings. It is necessary to search individually in each case. It's not so much the VDDQ TX (which supplies voltage directly to the controller and has nothing to do with timings) that matters, but the right VDD2. Not as important as CPU VDDQ.

It is necessary to test it, like everything related to the gearbox, with Y-CRUNCHER tests 14-18 with the processor in overclocking. Increasing overclocking increases VDD2. But it's not as important as **CPU VDDQ (TX).**Reference point**1.3-1.4V**

KARHU 10000%, 6800-32, IMC VDD2=**1.28V**

STOCK: Y-CRUNCHER, 6800-32, IMC VDD2=**1.26V**

OVERCLOCKING: Y-CRUNCHER, 6800-32, IMC VDD2=**1.35V**

We see that only 1.26-1.28V is enough for a carhu and a cruncher in stock, while even 1.34V is not enough for an overclocked processor for everyday use.

Interface information from Intel:

The DDR PHY connects the memory controller and external memory devices in the speed critical command path.
The DDR PHY implements the following functions:

- Calibration—the DDR PHY supports the JEDEC-specified steps to synchronize the memory timing between the controller and the SDRAM chips. The calibration algorithm is implemented in software.

- Memory device initialization—the DDR PHY performs the mode register write operations to initialize the devices. The DDR PHY handles re-initialization after a deep power down.
- Single-data-rate to double-data-rate conversion.

CPU VDDQ TX(akaTransmitter on Asus) - the range for MSI is not defined, the border is 1.45V. It is better not to exceed 1.45V for a constant. The main voltage must be selected. It is enough not to add or exceed the voltage by some 20mV in order to lose the stability of the system. This is especially true for high frequencies. The same story with SA, but the error may already be 50mV.

1.32V-FAIL https://i.ibb.co/dL9KT1T/VDDQ2-FAIL.png https://i.ibb.co/
1.25V-FAIL nBBVWDM/VDDQ-FAIL.png https://i.ibb.co/0jZByYh/7466-34-
1.29V-PASS cruncher-tx-1-29.png

Comment from*@odvolk10:*

“CPU VDDQ TX voltage is the most difficult voltage in DDR5 overclocking. Very much

affects stability in games like Call of Duty: Warzone, Cyberpunk 2077, Marvel's Spider-Man Remastered, as well as memory and synthetic tests. I repeat, it has a very strong effect, much more important than CPU VDD2 (MC), SA. The first thing I look for, if the memory is not stable - so this is it. According to experiments with EVGA, even 1.1V is enough for the 6400! The + of this board is that it exposes itself for different processes during training, almost always, if not always - correctly. To start overclocking, set (we will talk only about Hynix, if we consider Samsung, it is better not to follow this advice): DRAM VDD=1.55V, VDDQ=auto or 10% lower or equal to DRAM VDD, CPU VDD2=auto or = DRAM VDDQ. SA auto or 0.95 (for Hynix CR2) is enough even at 7000MHz."

Additional voltages:

> **CPU 1.05 (VCCIO CPU)**- AlwaysAuto. MSI range 0.6V - 2.0V.
> **CPU 1.8**- AlwaysAuto. MSI range 1.4V - 2.3V.
> **CPU AUX**– Range byMSI 1.4V - 2.3V. can be left in Auto and raised to 1.9V in overclocking 7000 and above.

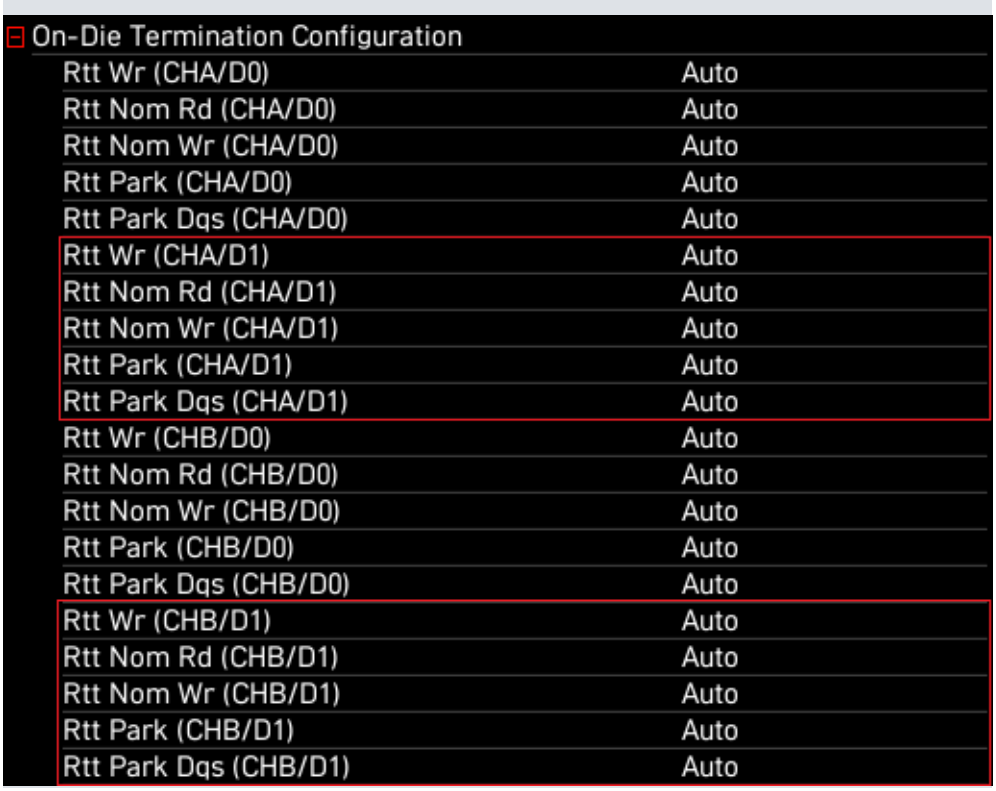
> **DRAM VPP (SWC)**- can be left inAuto and raise to 1.9V in overclocking 7000+.
> **PCH 0.82**- has nothing to do with memory. This is a chipset, you can carefully reduce it to minimum 0.6V. If the peripherals work and there is no BSOD, then it is stable. Helps to lower the temperature of the chipset a little. MSI range 0.6V - 1.4V.

Conclusions from *@anta777*:

DRAM VDD = set the voltage that suits us 1.40V (Jedec) / 1.435V (MSI) /
1.50V (Hynix) / 1.55V / 1.65V (on water)
2) DRAMVDDQ=0.94*DRAMVDD(my advice)/0.90*VDD(odvolk10)/0.95- 0.97*VDD(pakhtunov)/auto

3) CPU VDD2(MC)=DRAM VDDQ or auto/do not exceed 1.45V! or even 1.40V! (Igor's advice)
4) CPU VDDQ(TX)=min(1.1V-1.2V)
5) CPU SA=CPU VDDQ TX(Max's advice)/auto/0.95V(enough for 7000 CR2) For purists,
this option is also possible:
DRAM VDDQ=DRAM VDD-0.3V CPU VDD2=DRAM VDDQ CPU
AUX=1.85V
DRAM VPP=1.85V/1.908V/2.10V/2.135V

Resistances (On-Die Termination Configuration)



On-Die Termination Configuration	
Rtt Wr (CHA/D0)	Auto
Rtt Nom Rd (CHA/D0)	Auto
Rtt Nom Wr (CHA/D0)	Auto
Rtt Park (CHA/D0)	Auto
Rtt Park Dqs (CHA/D0)	Auto
Rtt Wr (CHA/D1)	Auto
Rtt Nom Rd (CHA/D1)	Auto
Rtt Nom Wr (CHA/D1)	Auto
Rtt Park (CHA/D1)	Auto
Rtt Park Dqs (CHA/D1)	Auto
Rtt Wr (CHB/D0)	Auto
Rtt Nom Rd (CHB/D0)	Auto
Rtt Nom Wr (CHB/D0)	Auto
Rtt Park (CHB/D0)	Auto
Rtt Park Dqs (CHB/D0)	Auto
Rtt Wr (CHB/D1)	Auto
Rtt Nom Rd (CHB/D1)	Auto
Rtt Nom Wr (CHB/D1)	Auto
Rtt Park (CHB/D1)	Auto
Rtt Park Dqs (CHB/D1)	Auto

DQS RTT PARK - step 240/120/80/60/40/34 (by Jedec off)
RTT PARK - step 240/120/80/60/40/34 (by Jedec off)
RTT WR - step 240/120/80/60/40/34 (according to Jedec 240 ohm)
RTT NOM WR - step 240/120/80/60/40/34 (according to Jedec 80 ohm)
RTT NOM RD - step 240/120/80/60/40/34 (according to Jedec 80 ohm)

This block should be touched as a last resort when tuning at frequencies higher than 7000MHz or do not touch at all. Profit from torsion resistance, at least for MSI is doubtful. MSI in current microcode revisions does not show real numbers.

It is necessary to look for the minimum values of WR/NOM RD/NOM WR for each and reduce to nebuta. Then try different configurations.

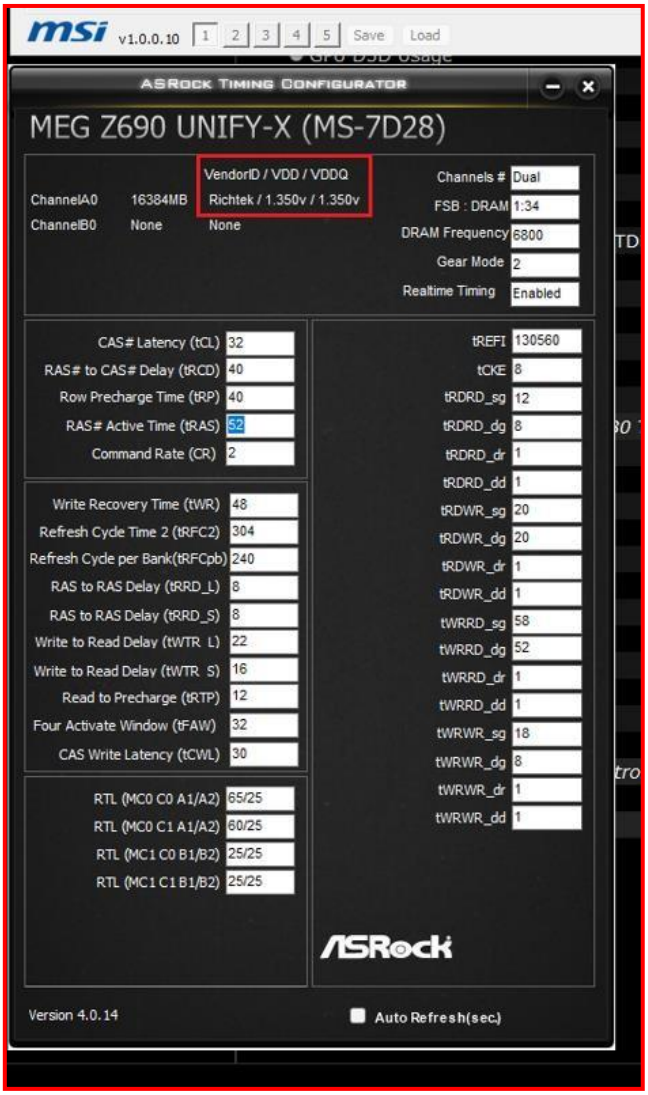
120/80/80; 120/60/60; 80/40/40; 80/34/34 and so on.

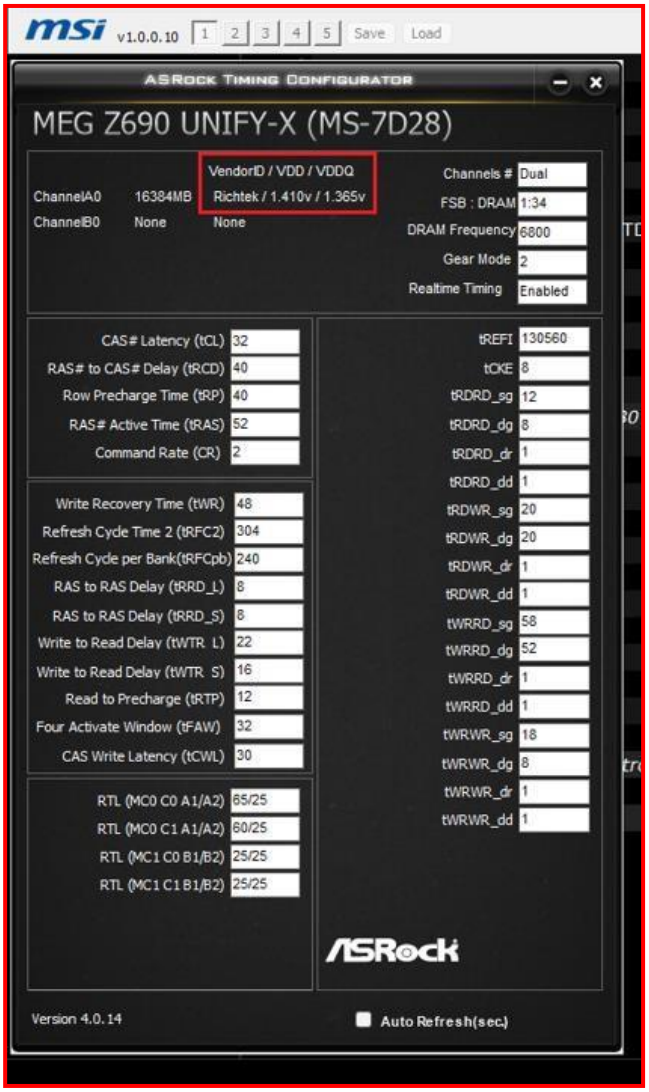
Setting example on ASUS APEX:

	from Shamino1978:
MC0/MC1	skew control/odts/
DQ RTT WR : 0/0	rtt WR 48
DQ RTT NOM RD : 48/48	rtt Nomrd 34
DQ RTT NOM WR : 48/48	rtt nom wr 34
DQ RTT PARK: 40/40	rtt park 34
DQ RTT PARK DQS: 34/34	rtt parkdqs 34
GroupA CA: 0/0	rtt ca group A 240
GroupA CS: 0/0	rtt cs group A 0
GroupA CK: 0/0	rtt ck group A 0
GroupB CA: 40/40	rtt ca group B 40
GroupB CS: 40/40	rtt cs group B 40
GroupB CK: 40/40	rtt ck group B 40
pull up: 34/34	Ron odt up/down: 34/34
pull-down: 34/34	

Finding the worst bar and adjusting voltages in Unlink mode

The task is to find the minimum DRAM VDD and DRAM VDDQ boot voltages for each bar in the DIMMA slot and then, based on this information, calibrate the voltages for each bar in Unlink mode for an already stable config. Optional.





1) Insert the first bar into DIMMA1 and reduce DRAM VDD by 0.01V (10mV) to the first file. We do the same with DRAM VDDQ
2) Insert the second bar into DIMMA1 and reduce DRAM VDD by 0.01V (10mV) to the first file. We do the same with DRAM VDDQ
3) We take the VDD of the worst bar, add 20-30mV to it and get a stable constant voltage. In my case, the minimum [DRAM VDD1=1.41V+0.3=1.44V]

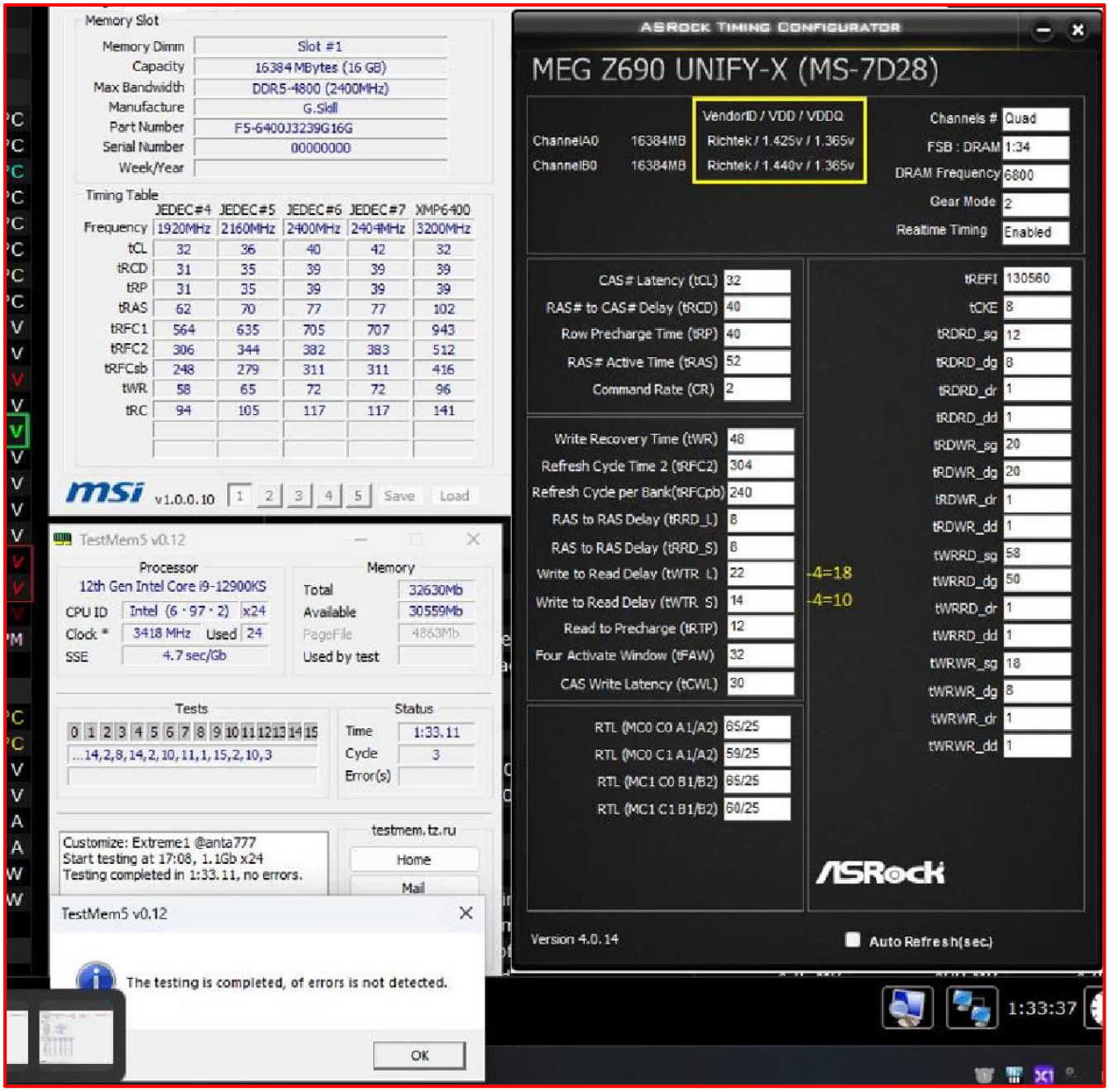
4) We subtract 15-30mV from the received voltage VDD and we get a stable VDD for our second (best) bar. [DRAM VDD2=1.44V-0.2=1.25V]
5) We set the voltage in Unlink mode. We pass the test. DRAM VDDQ set the same for two strips from the already tested config (with a margin). That is, we do not touch VDDQ. We are looking for a stub only for VDD.
6) Butovoe voltage DRAM VDDQ in both cases should be approximately the same level with an error of 10-20mV. We take the worst voltage and set it for two bars in Unlink mode.

7) We pass the test. If errors appear, increase it by 5-10mV. We pass the test. Don't forget that [DRAM VDDQ=CPU VDD2]

The result should be something like this:

DRAM Voltage Mode		[Unlink]
DRAM DIMMA1 Voltage	1.425V	1.425
DRAM DIMMB1 Voltage	1.440V	1.440
DRAM DIMMA1 VDDQ Voltage	1.370V	1.370
DRAM DIMMB1 VDDQ Voltage	1.370V	1.370
DRAM DIMMA1 VPP Voltage	1.800V	1.800
DRAM DIMMB1 VPP Voltage	1.800V	1.800

Note: when searching for different voltages for the strips, the BIOS does not allow you to set the difference more than 25 mV

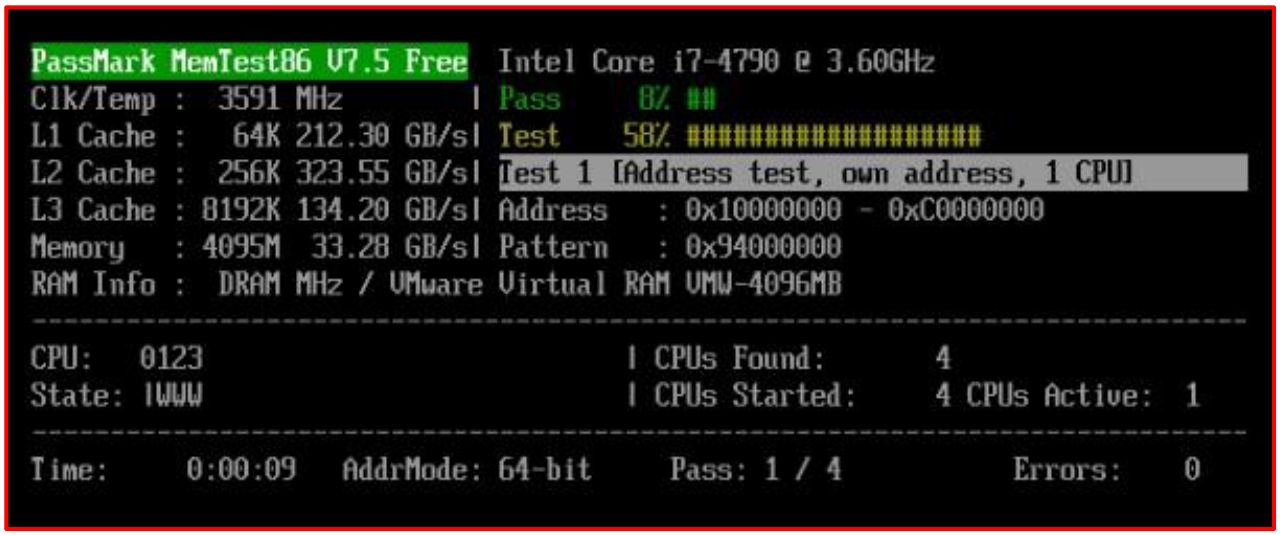


Basic tools for testing, monitoring, benchmarking

Basic Memory Testing Tools

MemTest86 V10 Pro

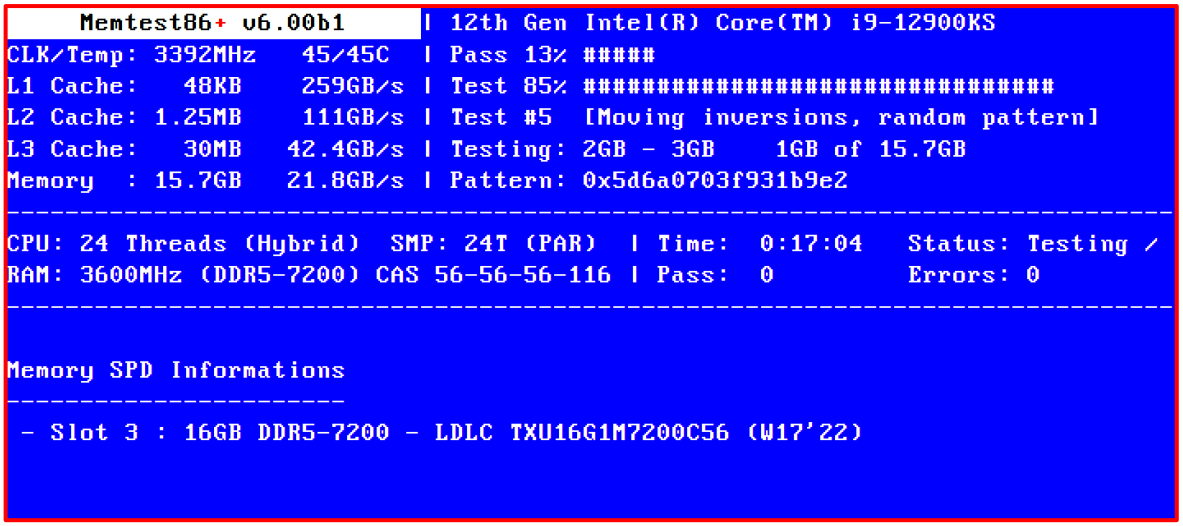
The main test that can be used as the only one to determine the 100% stability of the tuned memory. A total of 14 tests and 4 cycles, the total testing time is about 4 hours. In my opinion, it is enough to include tests 0-9 for 4 cycles (55 min). And at the final stage already TM5 Extreme.



This test also reveals hidden ECC errors at the very end.

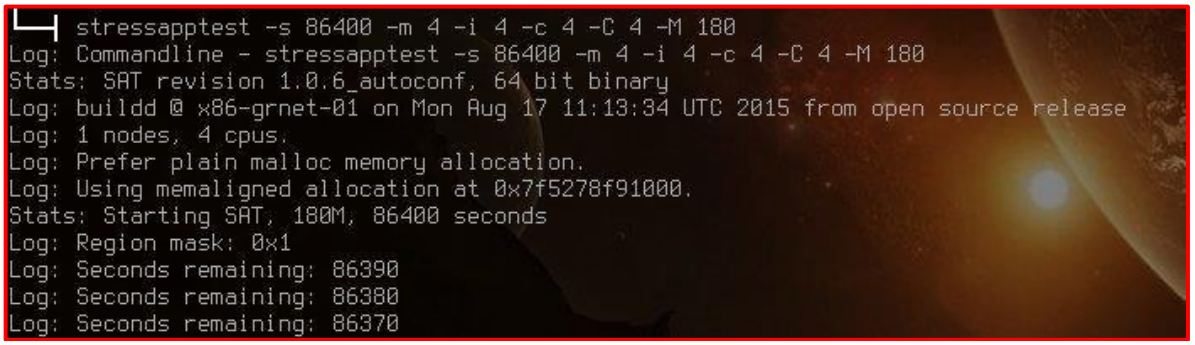
MemTest86+ V6

Free and simplified analogue of MemTest86 V10 Pro



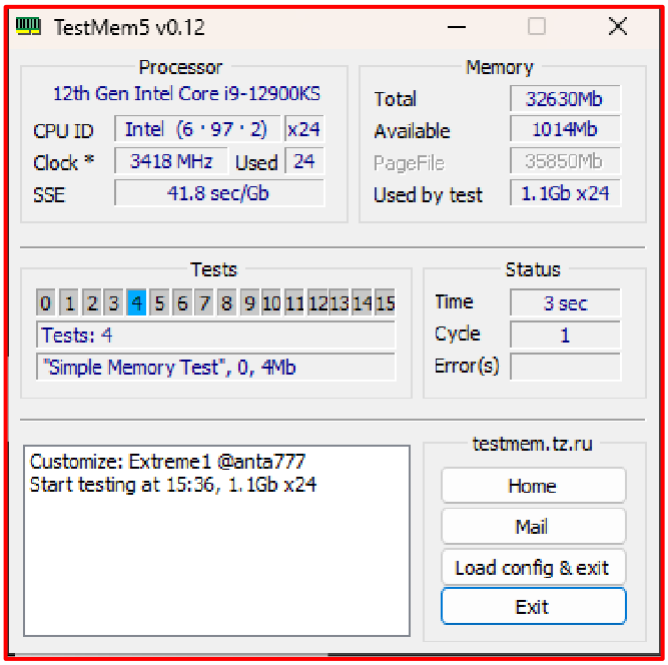
GSAT (Google Stressful Application Test)

Google's tool to check the health of the hardware devices in use. Under Linux, for advanced.



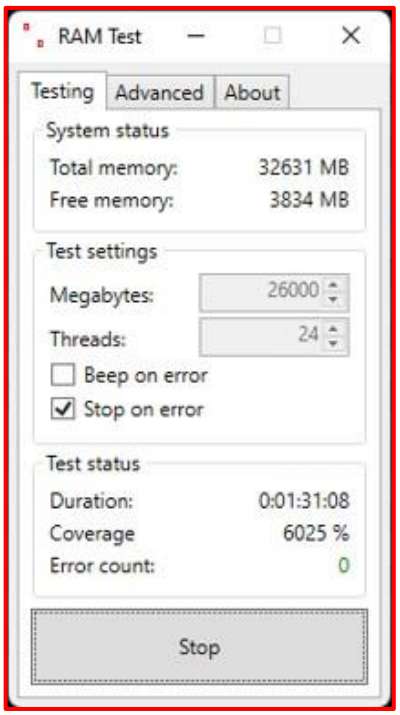
TestMem5 with Extreme config

It is also a basic and reliable memory testing tool. I do not consider other configs, since they reveal absolutely nothing.



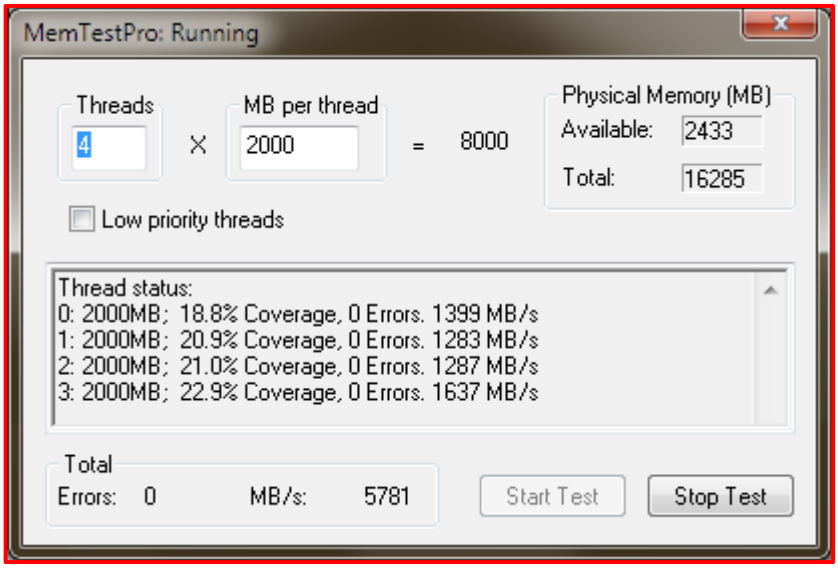
KARHU

As an addition to the above tests. Recommended 6000-10000%.



HCI memtest v7.0

The Windows version of HCI Memtest is a good test for both cache and memory loading at the same time.



The main tools for testing the voltage stability of the gearbox

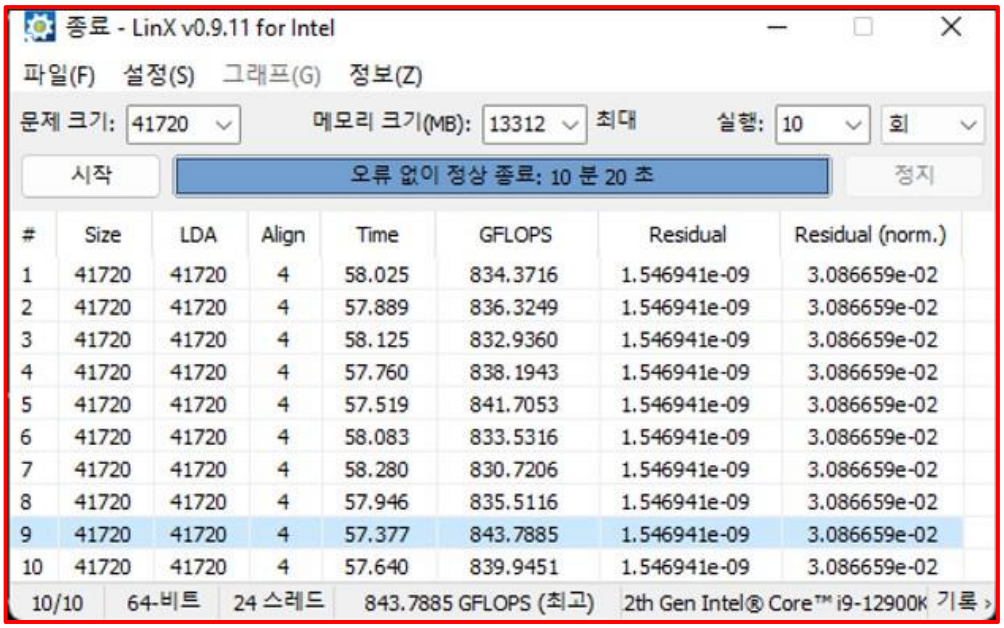
LinX 0.9.11 , 0.9.12

LinX v0.9.12 - Intel oneAPI Math Kernel Library업데이트 (버전:2022.0.2.92) LinX v0.9.11 - Intel oneAPI Math Kernel Library업데이트 (버전:2021.2.0.109)

Solid and reliable like a Swiss watch. But I personally prefer to useY-Cruncher , which is just as reliable, but eats 0.04-0.05V less.

It is necessary to clean Windows from all processes, so that their influence on the residuals is very large, and the residuals themselves may differ.

https://www.techpowerup.com/forums/threads/linpack-xtreme-released.247335/page-14#post-4305943
https://www.techpowerup.com/forums/threads/linpack-xtreme-released.247335 /page-14#post-4305943



#	Size	LDA	Align	Time	GFLOPS	Residual	Residual (norm.)
1	41720	41720	4	58.025	834.3716	1.546941e-09	3.086659e-02
2	41720	41720	4	57.889	836.3249	1.546941e-09	3.086659e-02
3	41720	41720	4	58.125	832.9360	1.546941e-09	3.086659e-02
4	41720	41720	4	57.760	838.1943	1.546941e-09	3.086659e-02
5	41720	41720	4	57.519	841.7053	1.546941e-09	3.086659e-02
6	41720	41720	4	58.083	833.5316	1.546941e-09	3.086659e-02
7	41720	41720	4	58.280	830.7206	1.546941e-09	3.086659e-02
8	41720	41720	4	57.946	835.5116	1.546941e-09	3.086659e-02
9	41720	41720	4	57.377	843.7885	1.546941e-09	3.086659e-02
10	41720	41720	4	57.640	839.9451	1.546941e-09	3.086659e-02

Y-Cruncher (set of tests 14-19)

Tests 11, 12, 13 - help in the initial assessment of the stability of the processor.
BKT-Basecase and Karatsuba's algorithm does not test anything. If the system drops on it, your business is very bad.
BBP– Bailey-Borwain-Pluff algorithm, calculationnth digit of pi. Initial test with AVX-2 instructions (floating point).
SFT-Small FFT, test with AVX-2 instructions (floating point). Almost identical to Prime95. Well loads percents, but is the second most important.

Tests 14-18 - test the stability of the processor in conjunction with the memory (KP, ring). Important in assessing the stability of the entire system.
FFTis the fast Fourier transform. InstructionsAVX-2 floating point. Exceptional memory. N32 - AVX-2 instructions (integers). Starting from it and down the list, it tests your percent (KP) in conjunction with memory. The ideal REFI/RFC check tool. Can draw a bug on an inflated ring.

N32-Classic NTT, 32-bit. Disabled in stock. We check tREFI / RFC for them. **N64**-
Classic NTT, 64-bit. Stock included.
HNT- same as above, but hybrid - mixed load. Shows instability as
processor, and CP. With an overclocked core frequency / lack of voltage on the VCORE / overestimated ring, it tends to put the system in a BSOD or draw an error. 3rd by

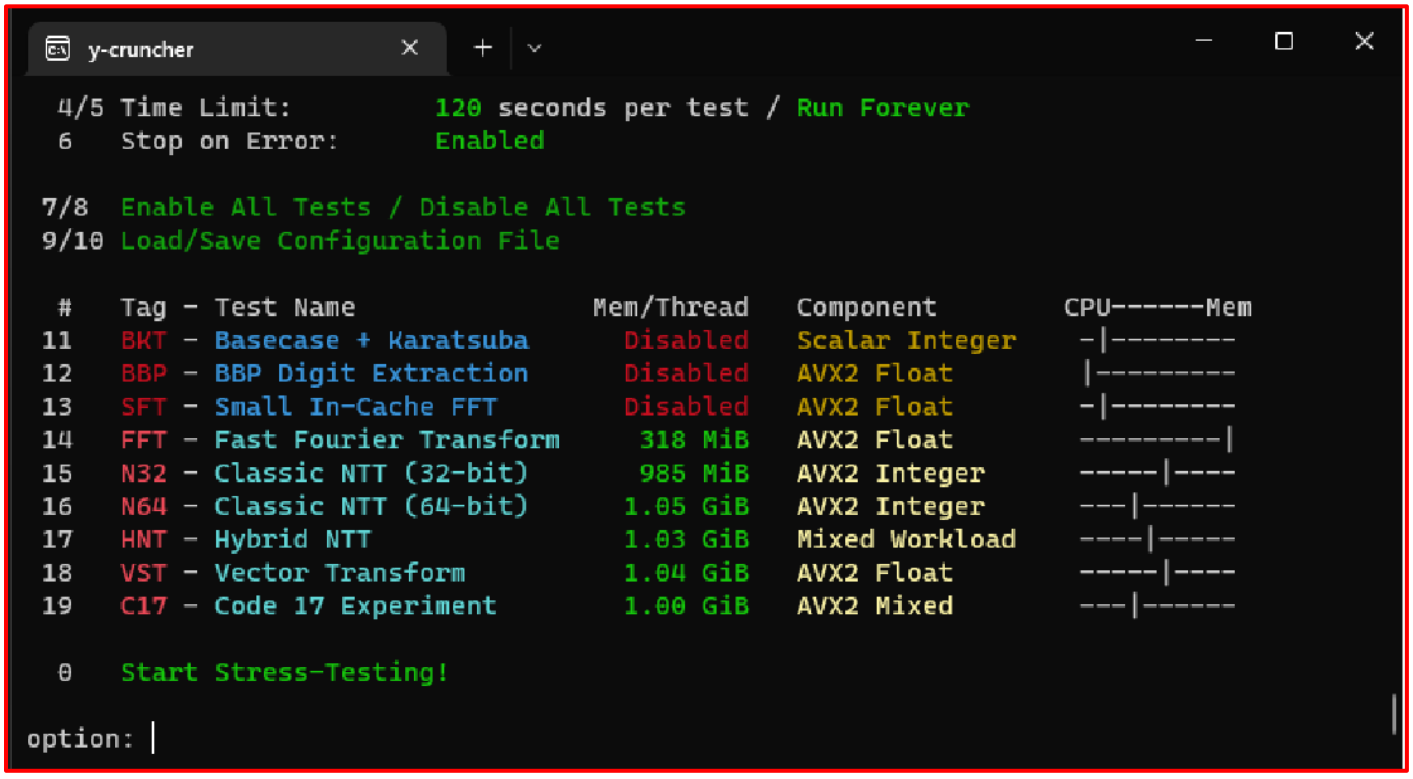
importance test after VST and SFT.
VST– vector transformation (floating point). The most important test of all the above. The load is similar to SFT, only now in conjunction with memory. drops
system very briskly and almost immediately.
It is also good for them to look for stable frequencies / VCORE, but after SFT. **C17**-
mixedAVX. Disabled.

All tests can be left in stock, nothing needs to be changed. We set the time to 60 seconds for each test. And at least 10 cycles is a 100% guarantee of your system's performance. You can determine the time for the test and the total test time in accordance with your tasks. If the computer is rendering, then 10 cycles will not be enough, and it may be necessary to increase the time for passing one test to 120 seconds or more.

Y-Cruncher helps to study your system and its potential very well, you need to learn to understand what gives the passage or failure of one or another test.

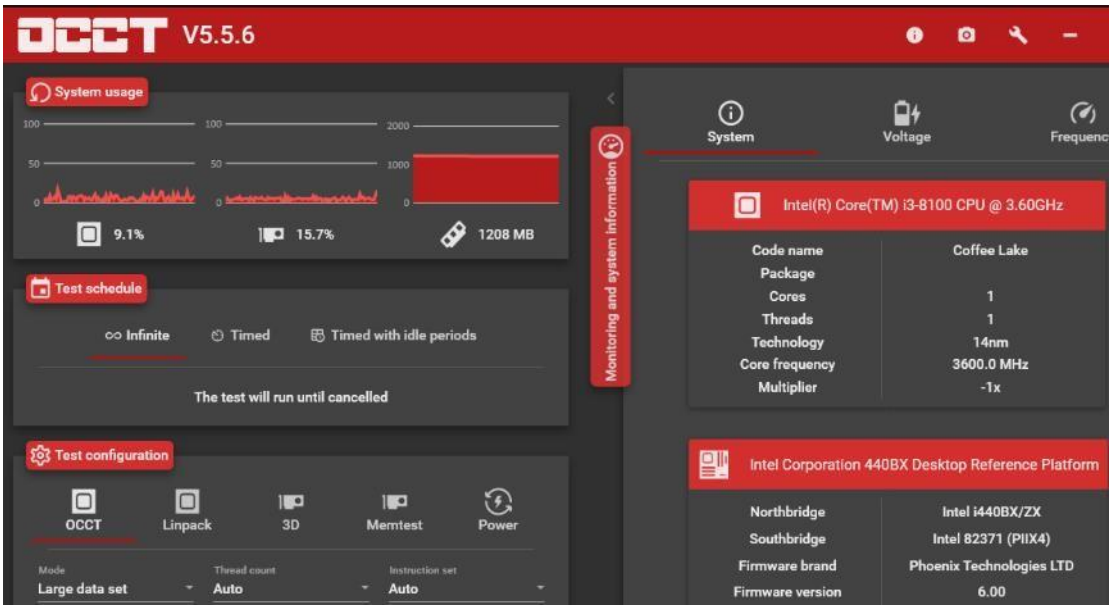
Bylink You can find explanations of the developer on the mat. parts.

Here he writes that the HNT, VST and C19 tests are not as important in practice as they were in 2009 at launch, but are very important now in terms of memory binding, I quote:
"For all practical purposes, these "novelty" algorithms are less important today than back in 2009 when y-cruncher first launched. Nowadays, these algorithms are becoming increasingly memory bound. So the quality of implementation with respect to memory usage matters more than the underlying math."



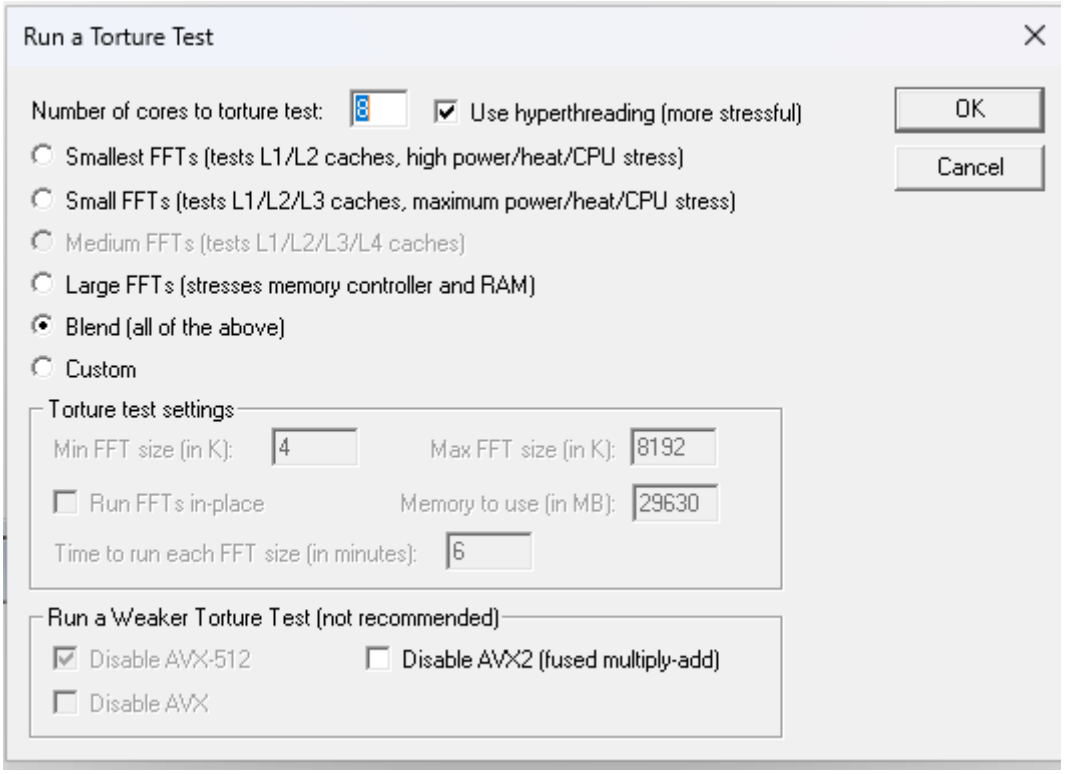
OCBASE/OCCT

There same where and LinX. I don't use it, but maybe it will make sense for someone.



PRIME 95

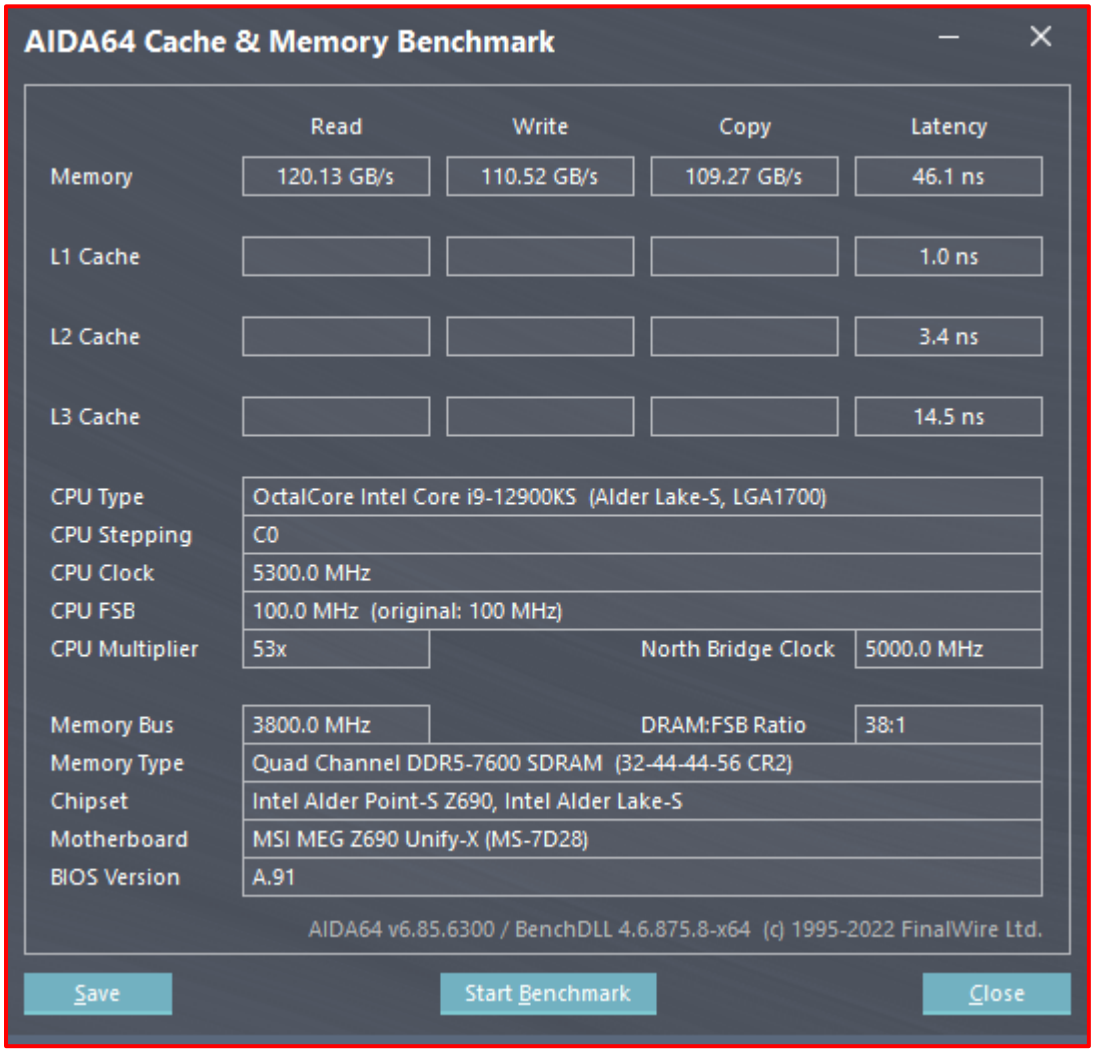
Mast have. Fries like links (Small FFT), but you can choose different configs. A very valuable tool that I almost forgot about.



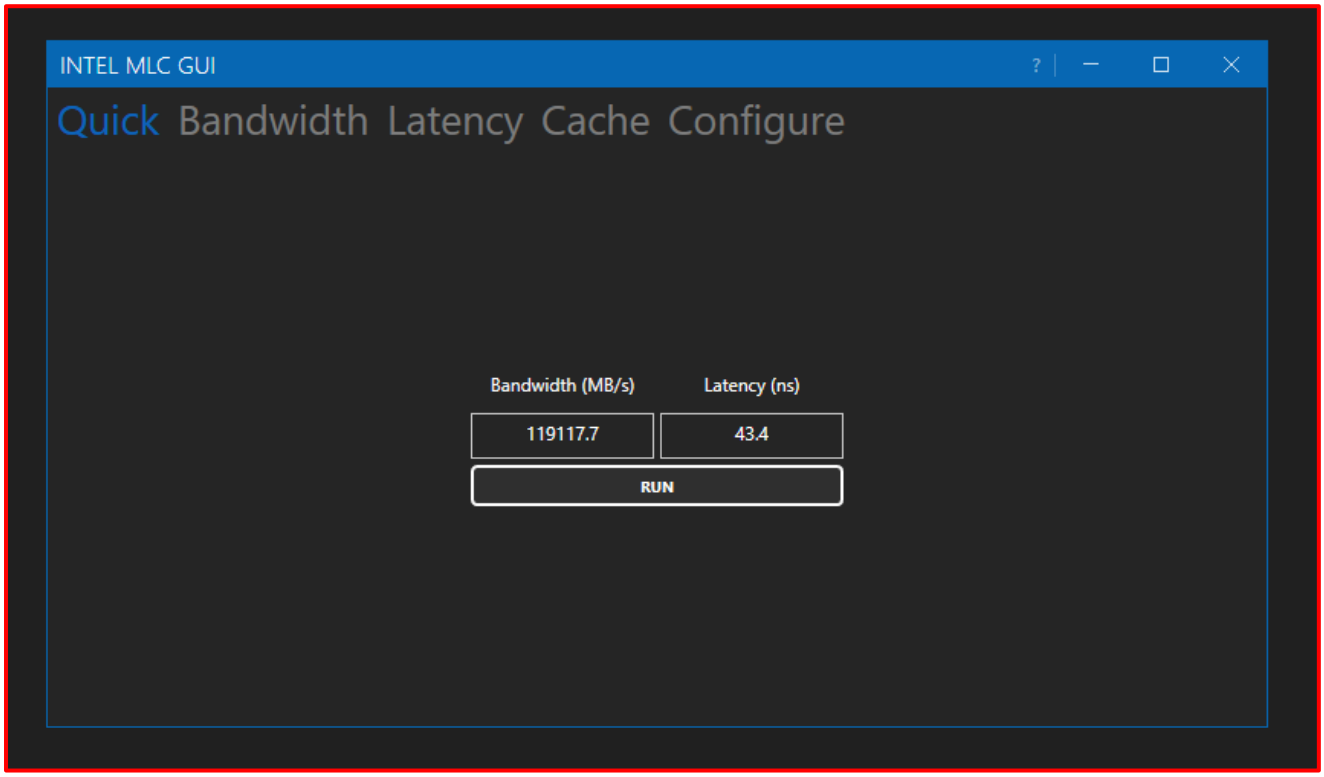
Basic tools for benches

AIDA EXTREME/BUSINESS (Cache and Memory Benchmark + Photoworxx)

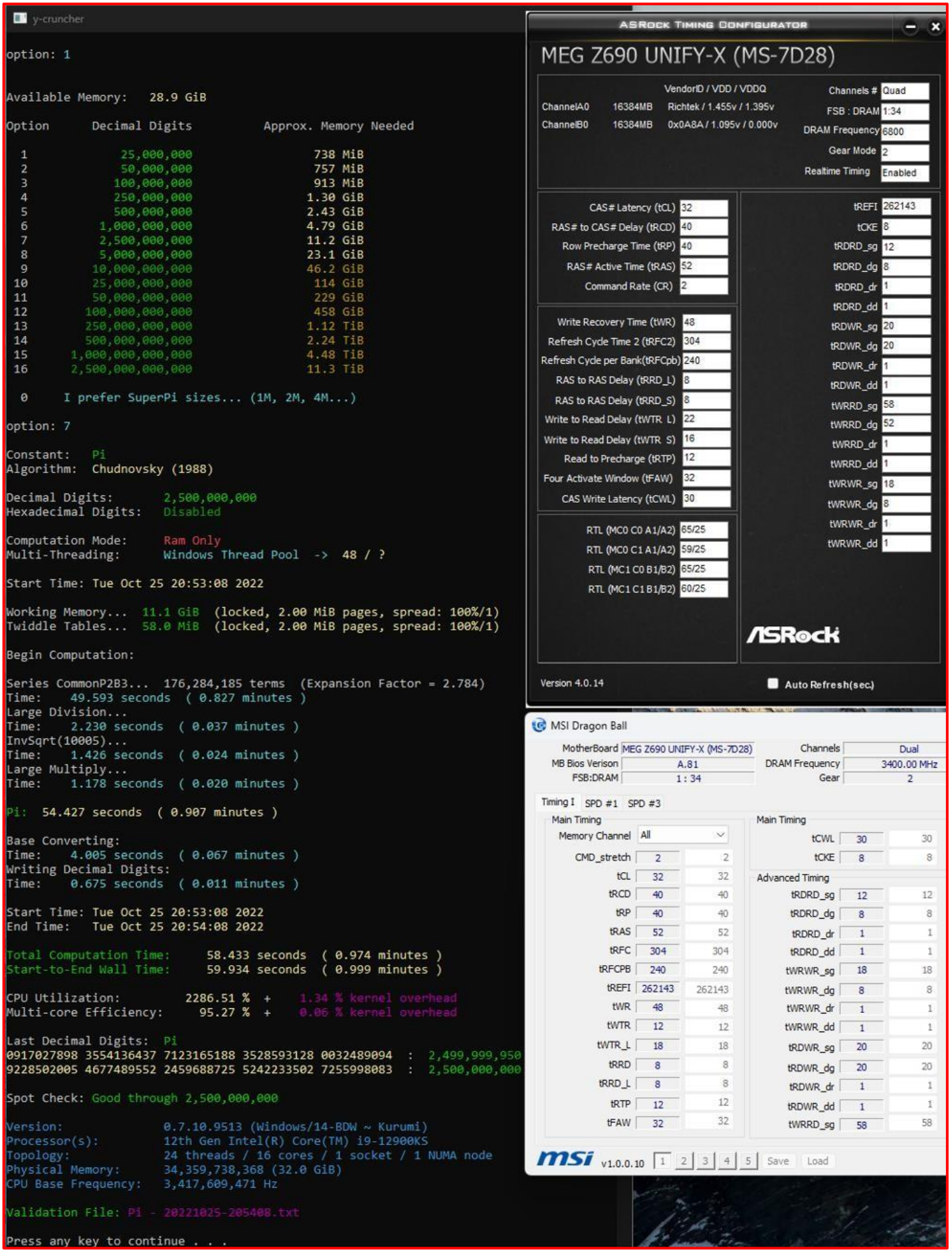
It is recommended to turn off the E-Cores and raise the ring to a stable maximum. With the cores enabled, we will see higher numbers on L1/L2/L3 but a loss in latency of about 2ns. The same goes for the Intel MLC.



INTEL MLC GUI (Quick + Latency)

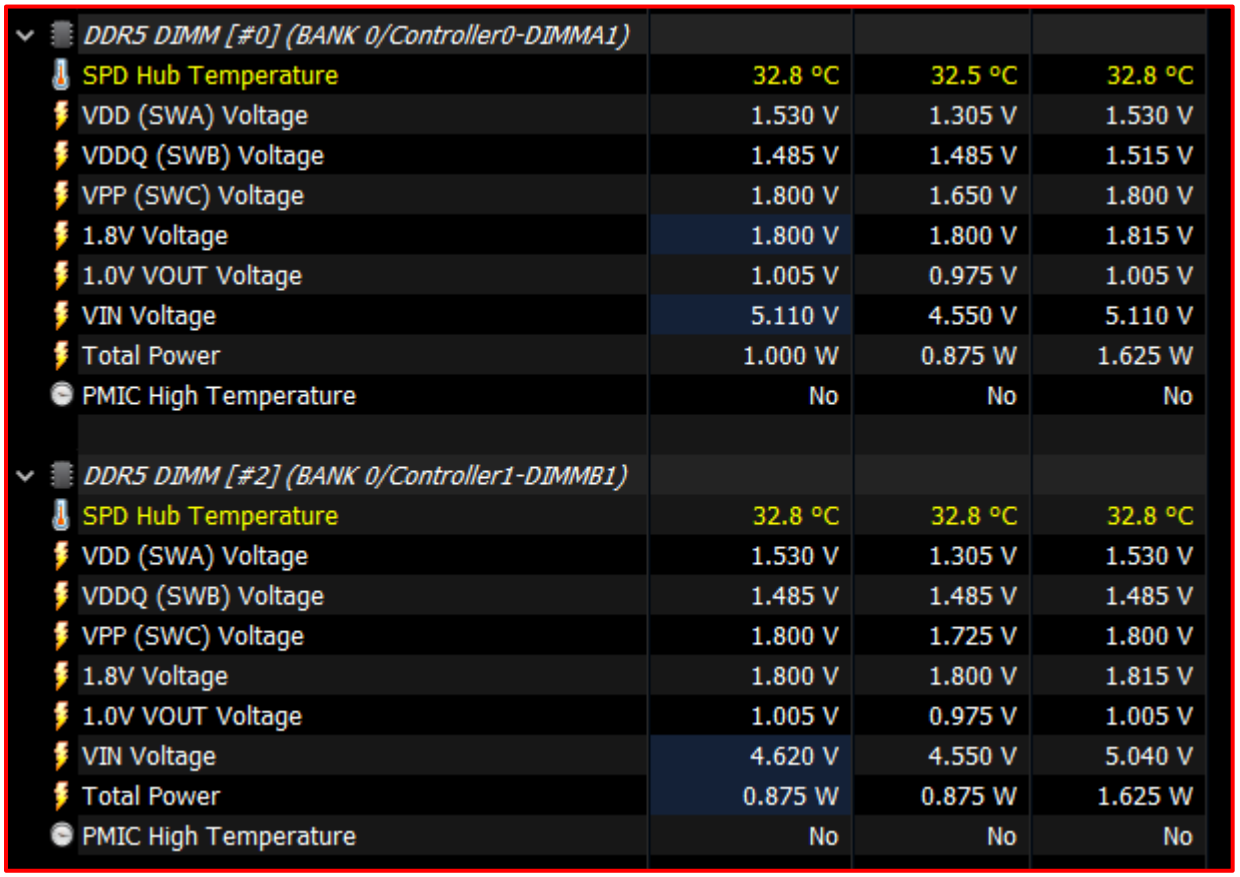


Y-Cruncher (Pi)



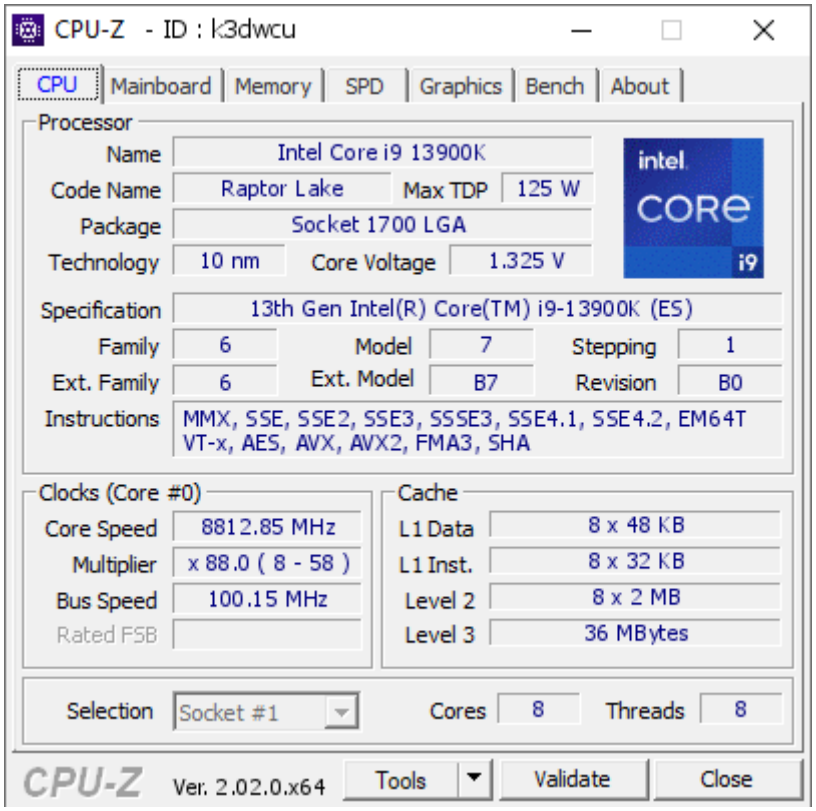
Basic monitoring tools

HWINFO64

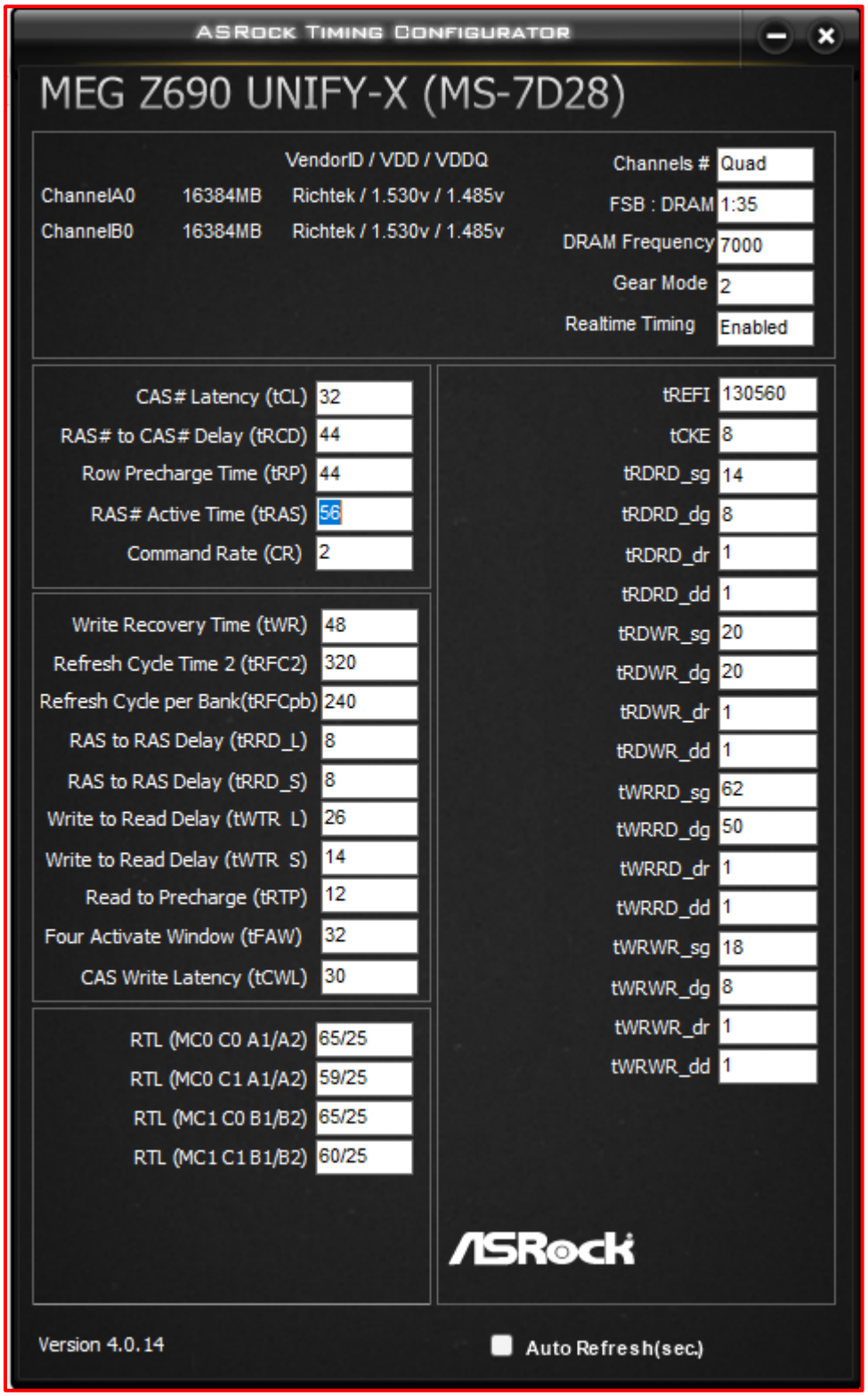


DDR5 DIMM [#0] (BANK 0/Controller0-DIMMA1)			
SPD Hub Temperature	32.8 °C	32.5 °C	32.8 °C
VDD (SWA) Voltage	1.530 V	1.305 V	1.530 V
VDDQ (SWB) Voltage	1.485 V	1.485 V	1.515 V
VPP (SWC) Voltage	1.800 V	1.650 V	1.800 V
1.8V Voltage	1.800 V	1.800 V	1.815 V
1.0V VOUT Voltage	1.005 V	0.975 V	1.005 V
VIN Voltage	5.110 V	4.550 V	5.110 V
Total Power	1.000 W	0.875 W	1.625 W
PMIC High Temperature	No	No	No
DDR5 DIMM [#2] (BANK 0/Controller1-DIMMB1)			
SPD Hub Temperature	32.8 °C	32.8 °C	32.8 °C
VDD (SWA) Voltage	1.530 V	1.305 V	1.530 V
VDDQ (SWB) Voltage	1.485 V	1.485 V	1.485 V
VPP (SWC) Voltage	1.800 V	1.725 V	1.800 V
1.8V Voltage	1.800 V	1.800 V	1.815 V
1.0V VOUT Voltage	1.005 V	0.975 V	1.005 V
VIN Voltage	4.620 V	4.550 V	5.040 V
Total Power	0.875 W	0.875 W	1.625 W
PMIC High Temperature	No	No	No

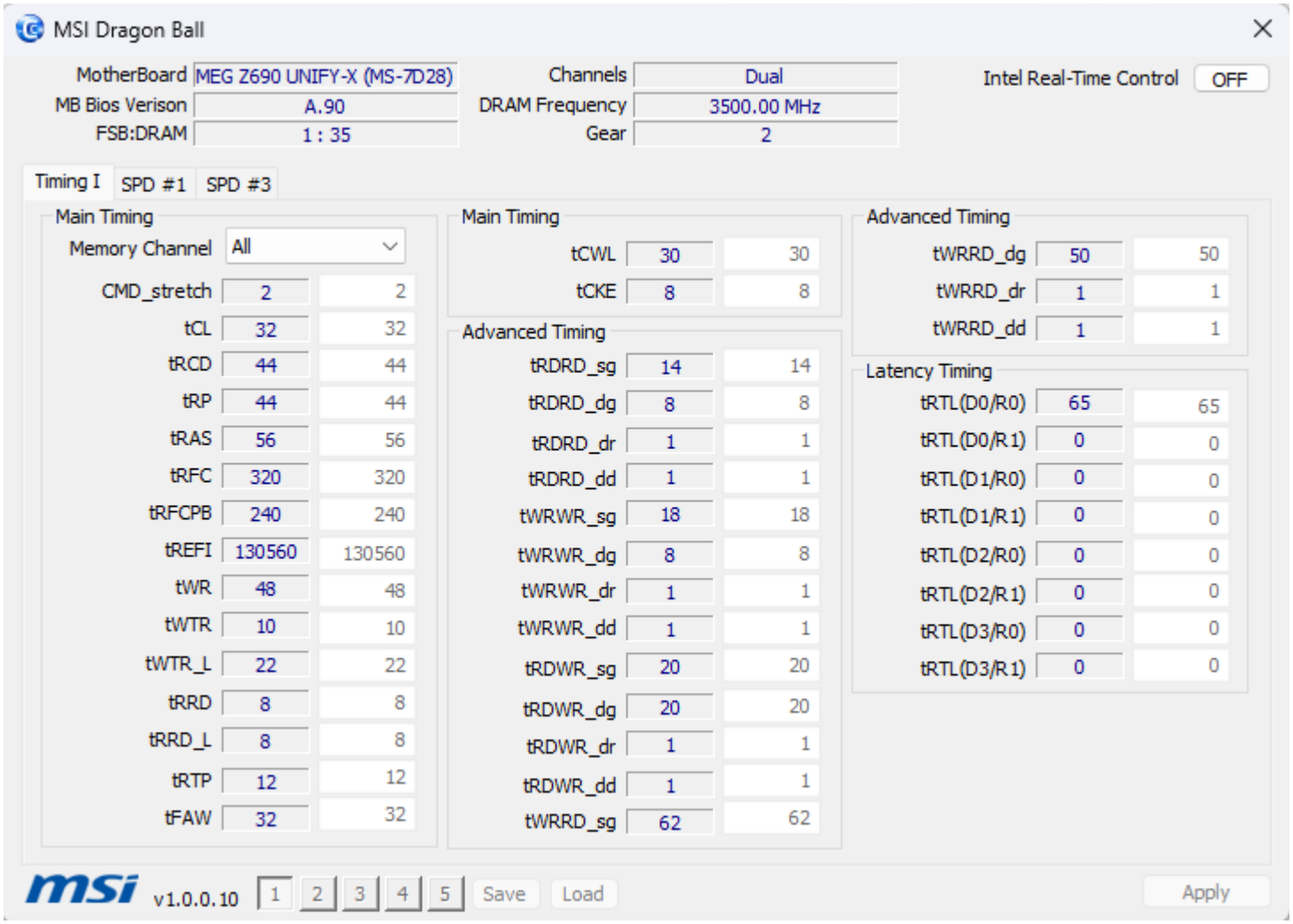
CPU-Z



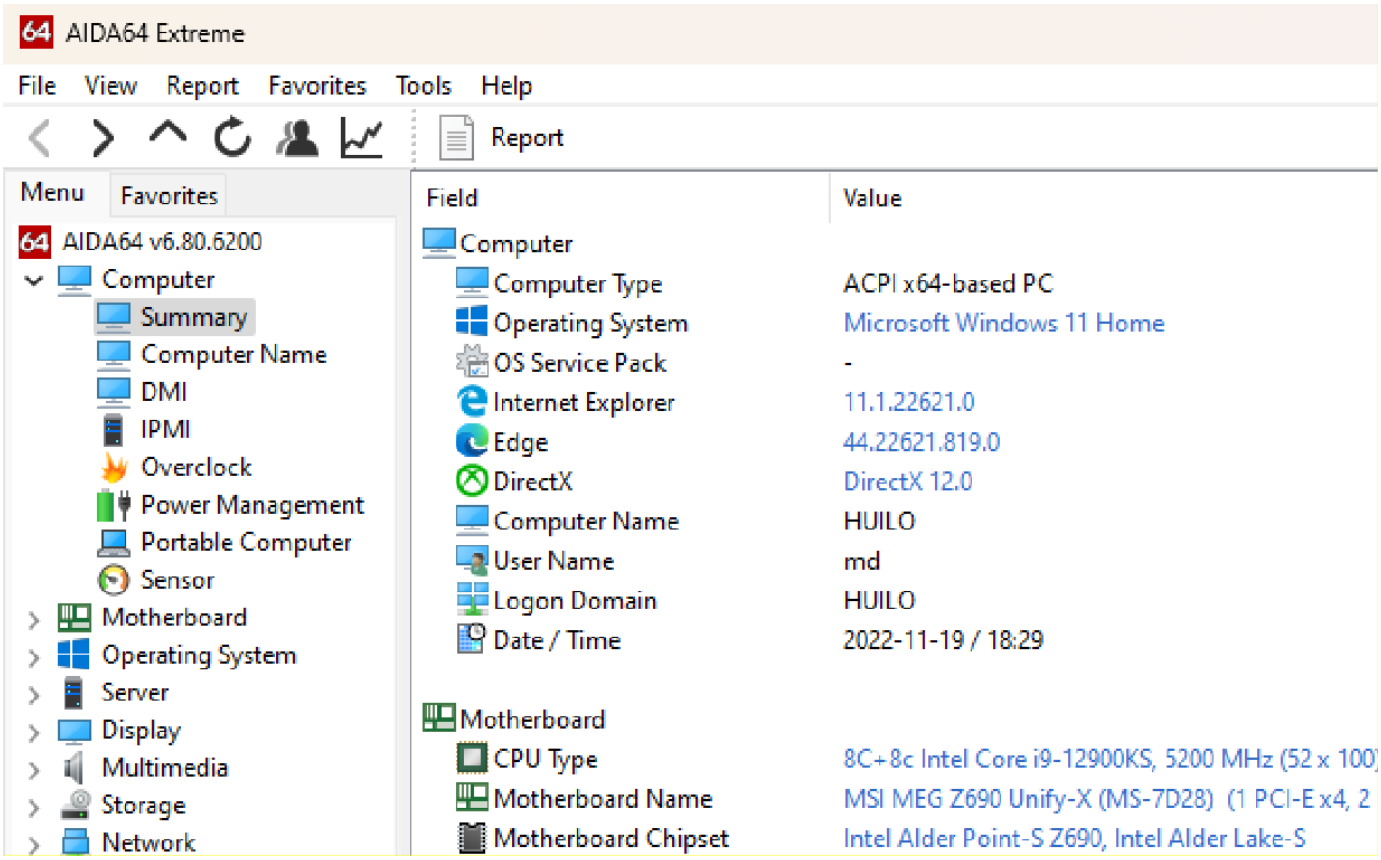
ASROCK TIMING CONFIGURATOR



MSI DRAGONBALL



AIDA EXTREME



Examples of setting M-DIE on Z690+ADL

https://www.overclock.net/threads/g-skill-6400-32-6800-32-1-365v-sa-0-92v-tx-1-1v.1801533/ https://www.overclock. net/threads/teamgroup-6400-32-2x16-6800-32-1-38v-1-42v-hynix-m-die.1802306/ https://www.overclock.net/threads/g-skill-6400- 32-6800-30-39-39-51-47-7ns-adl-m-die.1802501/ https://www.overclock.net/threads/oc-teamgroup-6400-6666-30-39-39- 51-6800-32-comparison.1803670/ https://www.overclock.net/threads/oc-teamgroup-6400-m-die-7000-32-unify-x.1803903/

A-DIE setup example on ADL+Z690

https://www.overclock.net/threads/oc-teamgroup-7600-7600-34-690-adl-44ns-mlc.1803693/ https://www.overclock.net/threads/oc-teamgroup-7600- 7200-32-690-adl-45-3ns-mlc.1803706/ https://www.overclock.net/threads/oc-teamgroup-7600-7400-32-690-adl-44-2ns-mlc.1803716/ https://www.overclock.net/threads/oc-teamgroup-7600-7600-32-690-adl-44-3ns-mlc.1803828/

Important notes and additional information

Comments from Chinese engineers (posted **https://forum.coolaler.com/viewtopic.php?p=17802293#p17802293**) @2500K, link to original post:

1. Disabling ECORE can help improve IMC and get higher overclocking frequency and overclocking stability. Overclocking DDR5 12th generation also has the characteristics of other Intel gen xx TH before. higher frequency, so when the memory cannot be debugged and cannot be stabilized, please set the CPU frequency and RING frequency to AUTO for troubleshooting, which can help to some extent. Memory temperature and CPU temperature will also challenge the upper limit and stability of OC memory, so pay attention to the temperature to ensure the stability of the OC, and when the memory parameters are tighter and lower, a lower temperature is required to ensure the OC memory

   temperature.
2. When overclocking DDR5 memory for the first time, it is initially recommended to select a suitable frequency for the usual work and have a general idea of the hardware on hand. Please do not set other people's parameters or archive without permission! ! ! (Any hardware system is unknown!!!! No absolute!!!!) Let's take the 6400MHz frequency of Hynix memory particles as an example (note magnesium light will be particularly difficult, please choose to reduce the frequency), we can first choose suitable. Set tCL, tRCD and tRP to e.g. 36 44 44 (friendly and stable to Hynix particles). Currently, we first set IMC VSA, IMC VDDQ and IMC VDD2 to AUTO, and fix the memory and memory VDDQ voltage. For example, timing is 1.4V , the second and third parameters are AUTO, and then a memory stability test is performed (recommended MT5. 0, Ramtest, TM5 1us). If an error is reported, we prioritize increasing or decreasing memory voltage (usually increasing voltage). If the error message continues to appear, the second consideration is CPU VDDQ, the third consideration is VDD2, and the fourth consideration is increasing or decreasing CPU VSA voltage. Under normal circumstances, the IMC voltage requirement is: CPU VDDQ > CPU VDD2 > CPU VSA. When the second and third parameters are set to AUTO, the memory test can be stably passed in the third consideration is VDD2 and the fourth consideration is to increase or decrease the CPU voltage VSA. Under normal circumstances, the IMC voltage requirement is: CPU VDDQ > CPU VDD2 > CPU VSA. When the second and third parameters are set to AUTO, the memory test can be stably passed in the third consideration is VDD2 and the fourth consideration is to increase or decrease the CPU voltage VSA. Under normal circumstances, the IMC voltage requirement is: CPU VDDQ > CPU VDD2 > CPU VSA. When the second and third parameters are set to AUTO, the memory test can be stably passed in

present time, and the parameters can be changed gradually (see previous memory options page) to reduce the maximum possible number of unknown errors and memory instability. If an error occurs after changing the settings, run the voltage cycle described above to make changes until they stabilize. After a certain acquaintance is recommended to try Songshen first for higher frequencies (for example, 6800 MHz, 7000 MHz, 7200 MHz) (Note: the memory frequency of the motherboard 4DIMM boards are weaker than 2DIMM motherboard). Memory system, IMC system, optimization motherboard, etc. . These uncertainties will indicate that the higher the frequency, the harder it is to stabilize it, so please be patient to try debug to reach the ideal frequency (no absolute memory stability test error, it can tell you where the problem is, be patient).

3. Pay attention, What voltage everyone IMC regulated V accordance With test. Some processors have better IMC voltage resistance and can work with higher voltages. Under normal circumstances, a 1.45V CPU VSA can run at almost any frequency and may be required in some specific cases. cases.Under pressure up to 1.5V, for example, when turned on at a particularly high frequency. For CPU VDDQ in most cases, 1.5V is sufficient, sometimes 1.51V, 1.52V may be required, it is not recommended to exceed 1.55V. CPU VDD2 is not recommended to exceed 1.45 V. In most cases, more than 1.45 V is a side effect and causes instability. As the CPU VSA voltage increases, CPU VDDQ, CPU VDD2 you can consider increasing the AUX voltage, according to the default is 1.8V, you can increase it to 1.85V (Note: it can exceed 1.85V, but 1.85V is enough in most cases) AUX voltage can help get more stable voltage CPU VSA, CPU VDDQ.
4. Please pay attention to the memory voltage, the memory can not withstand voltage (High voltage cannot be turned on or the voltage cannot be stabilized above a certain voltage) does not mean that the memory is no good! ! ! ! For example, level the voltage resistance of some memory is 1.4xV, this does not mean that it is bad, some green bars or other OC bars may be lit on 7400MHz and 7466MHz. fried chicken also can be 7000MHz and 7200MHz. Although the parameters are looser, it really can use lower voltage for high frequency loading and frying chicken, but, may not be able to achieve tighter synchronization due to lack of valid voltage. However, some 1.5xV chargers cannot achieve more than high load values and fried chicken, for example, but can be 7400 MHz, and fried chick can't be 7200MHz (regardless of how parameters are changed or voltage), That's why withstands voltage not high is equal to all absolutes. The pressure resistance is only a harder and lower setting on the same frequency, and the resistance to pressure will be different at different frequencies. That's why every sliver has its own characteristics, and it is correct to carry out reasonable collocation and debugging.

Required Formulas

tWR=tWRPRE-tCWL-8
tWTRL(auto)=tWRRDsg-tCWL-10 tWTRS(auto)=tWRRDdg-tCWL-10 tWRWR_sg=tCCDLx2=[tCCDLWR]
tWRPRE=tWR+tCWL+8
tXP=8 tRDPRE=tRTP tRAS=tRCD+tRTP
WTRL=WRWRsg according to JEDEC (since the BIOS always overestimates wtrs and wtrl by 2, this has remained since DDR4, then you can set WTRL=WRWRsg-2)
RDRDdr=8+RPRE WRWRdr=8+WPRE WRRDdr=6+RPRE RCDWR<=RCD

DRAM VDDQ = CPU VDD2 = DRAM VDD+4%~

CCDS=BL/2=16/2=8 tXPDLL=28
MRR- Mode register READ command period= max(14ns;16) MRW-Mode register WRITE command period= max(5ns;8)